

FMC2662 – 8-GSPS 12-bit Dual DAC FMC Module

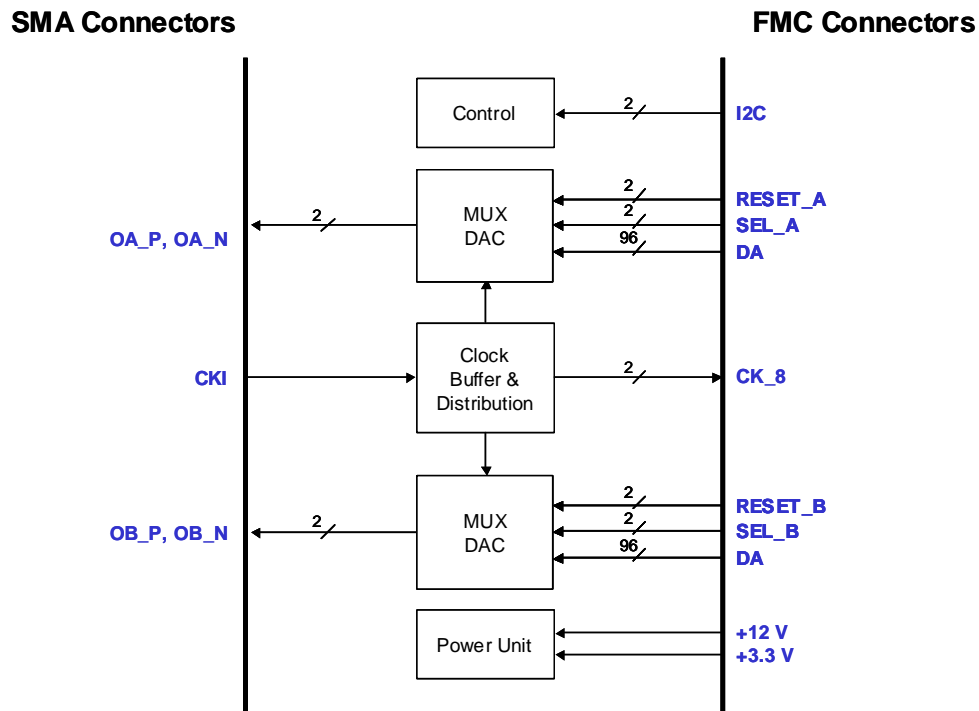
PRODUCT DESCRIPTION

The **FMC2662** module is equipped with two **Euvis MD662H** digital-to-analog converters (DAC's). At 8 GSPS, the module provides analog outputs with bandwidth from DC to 4 GHz (Nyquist bandwidth). The 96 LVDS pairs of digital data are fed through two FMC connectors, a high-pin-count (HPC) and a low-pin-count (LPC) connector. The digital data multiplexing ratio is 4:1 and the digital data rate is 2 Gb/s with the DAC's operating at 8 GSPS. Sampling window select (SEL's) and reset signals of the two DAC's can be independently controlled via the FMC connectors. The module includes two clock buffers to relax the need of high-power clock source. Both amplitudes and duty cycles of clock buffers can be programmed through I²C interface or use factory preset values.

KEY FEATURES

- Dual 12-bit DAC's
- 1 ~ 8 GSPS sampling rate
- On-board clock buffers with adjustable gain and duty cycle
- Power supplies needed from carrier: 12V and 3.3 V
- Compliant with Vita 57.1 standard

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min	Typical	Max	Unit
Operating Temperature	T_o		25		°C
Sampling Rate	f_{data}	1	8	8	GSPS
Clock Frequency	f_{CK}	0.5	4	4	GHz
Clock Input Power	P_{CK}	+3	+6	+10	dBm
Output Frequency ¹	f_{out}	0		4	GHz
Output Level ²	V_{out}	-635		0	mV
Output Power	P_{out}	-4		0	dBm
Output Residue Phase Noise ³	N_ϕ			-130	dBc/Hz
Output Port Return Loss	RL_{RF}		15		dB
Power Supply	V_{33}		+3.3		V
	I_{33}		250		mA
	V_{120}		+12		V
	I_{120}		1.2		A

¹Normal operation has usable bandwidth from DC to Nyquist bandwidth, 4 GHz, at 8 GSPS.

²If external 50-ohm loads are terminated to ground, the analog outputs will have voltage swings from ground to – 0.6 V with a common mode voltage of –0.3 V. If a positive analog output common mode level is desired, the external 50 ohm loads can be terminated to a positive voltage V_{pull} with a resultant analog output common mode voltage of $(V_{pull} - 0.6)/2$.

V_{pull} should not exceed 5 V.

³10 KHz offset

TERMINAL DESCRIPTION

Name	Function	I/O	Signal
CKI	Input Clock	I	RF
O_AP	CH A Analog Output Positive	O	RF
O_AN	CH A Analog Output Negative	O	RF
O_BP	CH B Analog Output Positive	O	RF
O_BN	CH B Analog Output Negative	O	RF
GND	Ground		DC
DA	48 LVDS Pairs of Digital Data Inputs for CH A	I	RF
DB	48 LVDS Pairs of Digital Data Inputs for CH B	I	RF
RESET_A	LVDS Pair inputs for CH A DAC Reset	I	RF
RESET_B	LVDS Pair inputs for CH B DAC Reset	I	RF
SEL_A	CH A DAC Sampling Window Select	I	DC
SEL_B	CH B DAC Sampling Window Select	I	DC
SCK	I2C Clock	I	RF
SDA	I2C Data	I/O	RF

SWITCHING CHARACTERISTICS

Parameter	Description	Min	Typ	Max	Units
Data, Reset, CK_8: LVDS Logic					
V _{IH}	Input Voltage High		1.4		V
V _{IL}	Input Voltage Low		1		V
I	Input driving current		2		mA
T _s	Setup time	0.2			ns
T _h	Hold time	0.2			ns
SEL: LVCOMS25 / LVCMOS18 Logic					
V _{IH}	Input Voltage High	1.5	2.5	2.8	V
V _{IL}	Input Voltage Low	-0.3	0	0.5	V
I	Input driving current		250		uA
I2C SDA, SCK: LVTTTL33 Logic					
Speed	Standard		100		KHz
	Fast		400		KHz
	High-Speed		3400		KHz
V _{IH}	Input Voltage High	2	3.3		V
V _{IL}	Input Voltage Low		0	1	V
I	Input driving current			±1	uA
C _{in}	Input Capacitance			2	pF
V _{Hys}	Input Hysteresis	0.3			V

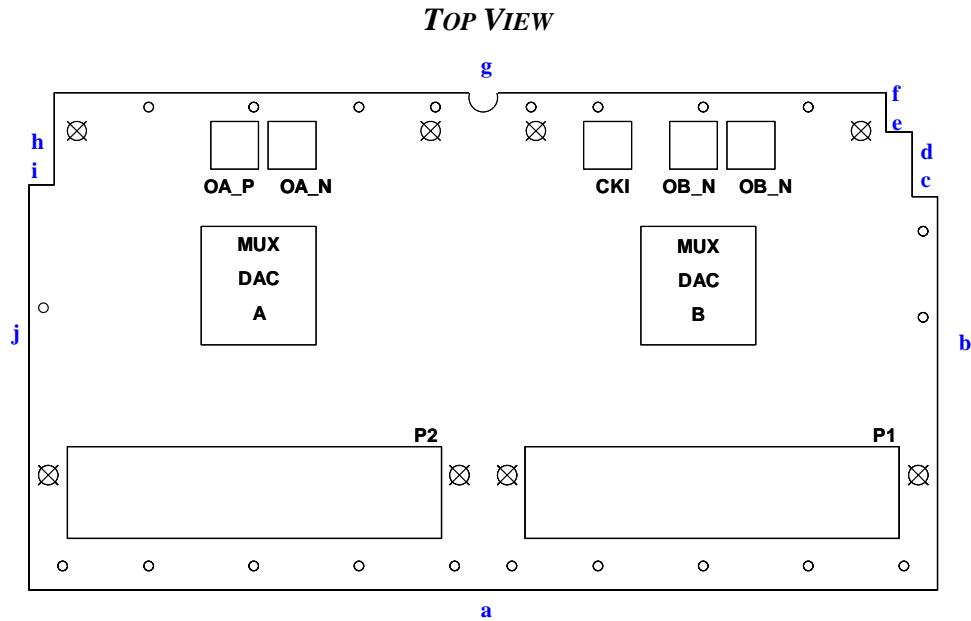
PIN ASSIGNMENTS

Signal Name	FMC Pin Name	
MDA_RESETP	LPC_LA06P	P2.C10
MDA_RESETN	LPC_LA06N	P2.C11
MDA_SEL1	LPC_LA01P	P2.D8
MDA_SEL2	LPC_LA01N	P2.D9
MDB_RESETP	HPC_HA02P	P1.K7
MDB_RESETN	HPC_HA02N	P1.K8
MDB_SEL1	HPC_HA03P	P1.J6
MDB_SEL2	HPC_HA03N	P1.J7
CKD8FP	HPC_CLK00P	P1.H4
CKD8FN	HPC_CLK00N	P1.H5
+12V	12P0V	P1.C35
	12P0V	P1.C37
	12P0V	P2.C35
	12P0V	P2.C37
+3.3V	3P3V	P1.C39
	3P3VAUX	P1.D32
	3P3V	P1.D36
	3P3V	P1.D38
	3P3V	P1.D40
	3P3V	P2.C39
	3P3VAUX	P2.D32
	3P3V	P2.D36
	3P3V	P2.D38
3P3V	P2.D40	

MUXDAC A Data	FMC Pin		MUXDAC A Data	FMC Pin		MUXDAC A Data	FMC Pin	
A11	LPC_LA32P	P2.H37	A7	LPC_LA17P	P2.D20	A3	HPC_LA06P	P1.C10
	LPC_LA32N	P2.H38		LPC_LA17N	P2.D21		HPC_LA06N	P1.C11
B11	LPC_LA33P	P2.G36	B7	LPC_LA14P	P2.C18	B3	HPC_LA01P	P1.D8
	LPC_LA33N	P2.G37		LPC_LA14N	P2.C19		HPC_LA01N	P1.D9
C11	LPC_LA30P	P2.H34	C7	LPC_LA13P	P2.D17	C3	HPC_LA00P	P1.G6
	LPC_LA30N	P2.H35		LPC_LA13N	P2.D18		HPC_LA00N	P1.G7
D11	LPC_LA31P	P2.G33	D7	LPC_LA15P	P2.H19	D3	HPC_LA05P	P1.D11
	LPC_LA31N	P2.G34		LPC_LA15N	P2.H20		HPC_LA05N	P1.D12
A10	LPC_LA28P	P2.H31	A6	LPC_LA16P	P2.G18	A2	HPC_LA03P	P1.G9
	LPC_LA28N	P2.H32		LPC_LA16N	P2.G19		HPC_LA03N	P1.G10
B10	LPC_LA29P	P2.G30	B6	LPC_LA11P	P2.H16	B2	HPC_LA04P	P1.H10
	LPC_LA29N	P2.G31		LPC_LA11N	P2.H17		HPC_LA04N	P1.H11
C10	LPC_LA24P	P2.H28	C6	LPC_LA12P	P2.G15	C2	HPC_LA08P	P1.G12
	LPC_LA24N	P2.H29		LPC_LA12N	P2.G16		HPC_LA08N	P1.G13
D10	LPC_LA25P	P2.G27	D6	LPC_LA09P	P2.D14	D2	HPC_LA07P	P1.H13
	LPC_LA25N	P2.G28		LPC_LA09N	P2.D15		HPC_LA07N	P1.H14
A9	LPC_LA18P	P2.C22	A5	LPC_LA10P	P2.C14	A1	HPC_HA05P	P1.E6
	LPC_LA18N	P2.C23		LPC_LA10N	P2.C15		HPC_HA05N	P1.E7
B9	LPC_LA23P	P2.D23	B5	LPC_LA07P	P2.H13	B1	HPC_HA04P	P1.F7
	LPC_LA23N	P2.D24		LPC_LA07N	P2.H14		HPC_HA04N	P1.F8
C9	LPC_LA21P	P2.H25	C5	LPC_LA08P	P2.G12	C1	HPC_HA09P	P1.E9
	LPC_LA21N	P2.H26		LPC_LA08N	P2.G13		HPC_HA09N	P1.E10
D9	LPC_LA22P	P2.G24	D5	LPC_LA05P	P2.D11	D1	HPC_HA08P	P1.F10
	LPC_LA22N	P2.G25		LPC_LA05N	P2.D12		HPC_HA08N	P1.F11
A8	LPC_LA26P	P2.D26	A4	LPC_LA04P	P2.H10	A0	HPC_HA07P	P1.J9
	LPC_LA26N	P2.D27		LPC_LA04N	P2.H11		HPC_HA07N	P1.J10
B8	LPC_LA27P	P2.C26	B4	LPC_LA03P	P2.G9	B0	HPC_HA06P	P1.K10
	LPC_LA27N	P2.C27		LPC_LA03N	P2.G10		HPC_HA06N	P1.K11
C8	LPC_LA19P	P2.H22	C4	LPC_LA02P	P2.H7	C0	HPC_HA13P	P1.E12
	LPC_LA19N	P2.H23		LPC_LA02N	P2.H8		HPC_HA13N	P1.E13
D8	LPC_LA20P	P2.G21	D4	LPC_LA00P	P2.G6	D0	HPC_HA12P	P1.F13
	LPC_LA20N	P2.G22		LPC_LA00N	P2.G7		HPC_HA12N	P1.F14

MUXDAC B Data	FMC Pin		MUXDAC B Data	FMC Pin		MUXDAC B Data	FMC Pin	
A11	HPC_HB17P	P1.K37	A7	HPC_LA21P	P1.H25	A3	HPC_LA15P	P1.H19
	HPC_HB17N	P1.K38		HPC_LA21N	P1.H26		HPC_LA15N	P1.H20
B11	HPC_HB18P	P1.J36	B7	HPC_LA22P	P1.G24	B3	HPC_LA16P	P1.G18
	HPC_HB18N	P1.J37		HPC_LA22N	P1.G25		HPC_LA16N	P1.G19
C11	HPC_HB16P	P1.F34	C7	HPC_LA23P	P1.D23	C3	HPC_LA14P	P1.C18
	HPC_HB16N	P1.F35		HPC_LA23N	P1.D24		HPC_LA14N	P1.C19
D11	HPC_HB19P	P1.E33	D7	HPC_LA17P	P1.D20	D3	HPC_LA13P	P1.D17
	HPC_HB19N	P1.E34		HPC_LA17N	P1.D21		HPC_LA13N	P1.D18
A10	HPC_HB14P	P1.K34	A6	HPC_HA23P	P1.K22	A2	HPC_LA11P	P1.H16
	HPC_HB14N	P1.K35		HPC_HA23N	P1.K23		HPC_LA11N	P1.H17
B10	HPC_HB15P	P1.J33	B6	HPC_HA22P	P1.J21	B2	HPC_LA12P	P1.G15
	HPC_HB15N	P1.J34		HPC_HA22N	P1.J22		HPC_LA12N	P1.G16
C10	HPC_HB12P	P1.F31	C6	HPC_HA19P	P1.F19	C2	HPC_LA09P	P1.D14
	HPC_HB12N	P1.F32		HPC_HA19N	P1.F20		HPC_LA09N	P1.D15
D10	HPC_HB13P	P1.E30	D6	HPC_HA20P	P1.E18	D2	HPC_LA10P	P1.C14
	HPC_HB13N	P1.E31		HPC_HA20N	P1.E19		HPC_LA10N	P1.C15
A9	HPC_HB10P	P1.K31	A5	HPC_HA21P	P1.K19	A1	HPC_LA25P	P1.G27
	HPC_HB10N	P1.K32		HPC_HA21N	P1.K20		HPC_LA25N	P1.G28
B9	HPC_HB11P	P1.J30	B5	HPC_HA18P	P1.J18	B1	HPC_LA24P	P1.H28
	HPC_HB11N	P1.J31		HPC_HA18N	P1.J19		HPC_LA24N	P1.H29
C9	HPC_HB08P	P1.F28	C5	HPC_HA17P	P1.K16	C1	HPC_LA29P	P1.G30
	HPC_HB08N	P1.F29		HPC_HA17N	P1.K17		HPC_LA29N	P1.G31
D9	HPC_HB09P	P1.E27	D5	HPC_HA15P	P1.F16	D1	HPC_LA28P	P1.H31
	HPC_HB09N	P1.E28		HPC_HA15N	P1.F17		HPC_LA28N	P1.H32
A8	HPC_HB06P	P1.K28	A4	HPC_HA14P	P1.J15	A0	HPC_LA31P	P1.G33
	HPC_HB06N	P1.K29		HPC_HA14N	P1.J16		HPC_LA31N	P1.G34
B8	HPC_HB07P	P1.J27	B4	HPC_HA11P	P1.J12	B0	HPC_LA30P	P1.H34
	HPC_HB07N	P1.J28		HPC_HA11N	P1.J13		HPC_LA30N	P1.H35
C8	HPC_HB00P	P1.K25	C4	HPC_HA10P	P1.K13	C0	HPC_LA33P	P1.G36
	HPC_HB00N	P1.K26		HPC_HA10N	P1.K14		HPC_LA33N	P1.G37
D8	HPC_HB01P	P1.J24	D4	HPC_HA16P	P1.E15	D0	HPC_LA32P	P1.H37
	HPC_HB01N	P1.J25		HPC_HA16N	P1.E16		HPC_LA32N	P1.H38

BOARD OUTLINE AND DIMENSIONS:



P1 is the primary HPC connector and P2 is the LPC connector. All dimensions use the bottom left corner of the board as the origin. All dimensions are in millimeters (mm). Board thickness is 1.62 mm.

Board Edge Lengths

Edge	Length	Edge	Length	Edge	Length
a	139	b	61.7	c	2.4
d	9.1	e	2.1	f	8
g	131.3	h	21.9	i	3
j	56.9	Width	139	Height	78.8

⊗ **FMC Connector Mount Hole Locations (x, y)**

73, 18.4	136, 18.4	3, 18.4	66, 18.4
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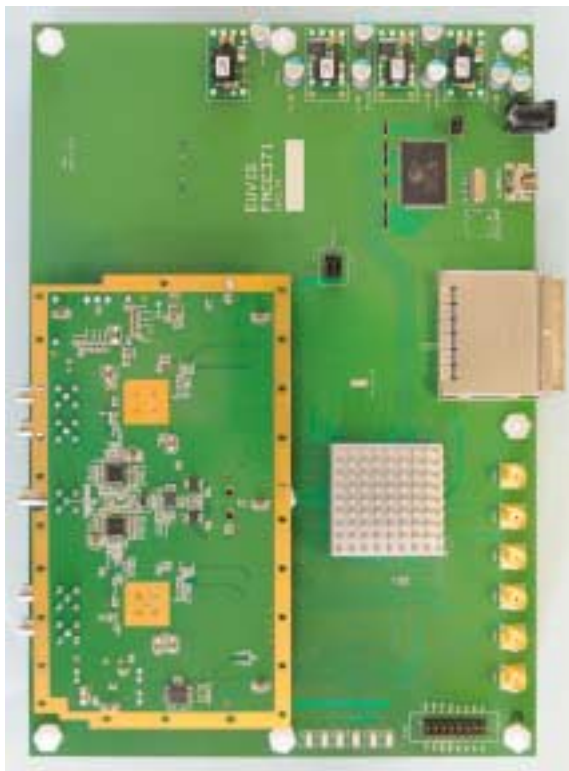
SMA Locations (x, y)

CKI	68.3, 68		
OA_P	37.0, 68	OB_P	98.8, 68
OA_N	47.4, 68	OB_N	109.2, 68

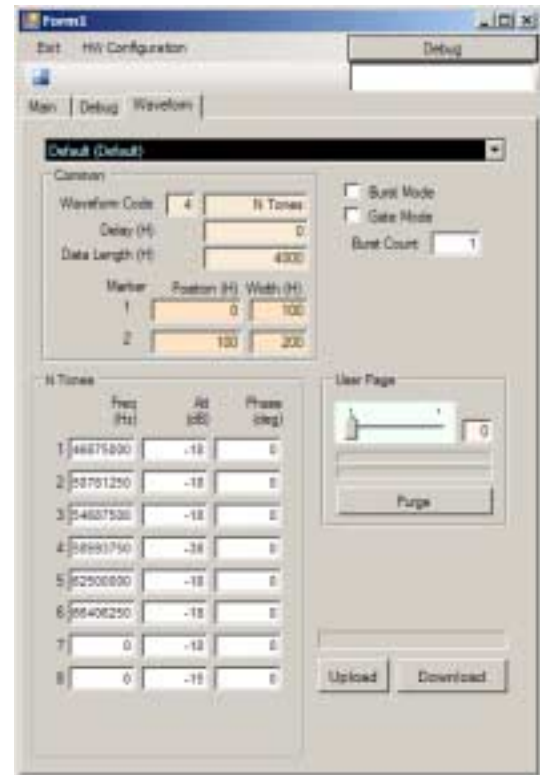
TEST SETUP

In applications, FMC2662 requires a VITA 57.1-compliant carrier board to provide all digital data, DAC controls, I²C signal, and DC powers via FMC connectors. The carrier must provide two power supplies, +12V and +3.3V, with minimum current capacities of 1A and 500mA respectively. Digital data and DAC resets are in LVDS pairs. The DAC timing selects and return-to-zero mode select are single-ended LVCMOS25. The carrier board can be an advanced FPGA evaluation board, such as Xilinx VC707, with proper configurations.

The FMC module is tested using Euvis carrier FMCC371 as shown in following figure. The carrier consists of a Xilinx XC6VLX130T, a USB controller, and power modules. In the test setup, the carrier is controlled by a PC host via the USB interface. The carrier can store up to 2 x 512 K words of data in memory. The maximum data length is 64 us at 4 GSPS for each channel. Several built-in waveforms are available as in our AWG's GUI. Waveform generation and download are performed in GUI.



USB
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