FMC2653 – 4-GSPS 12-bit Dual DAC FMC Module

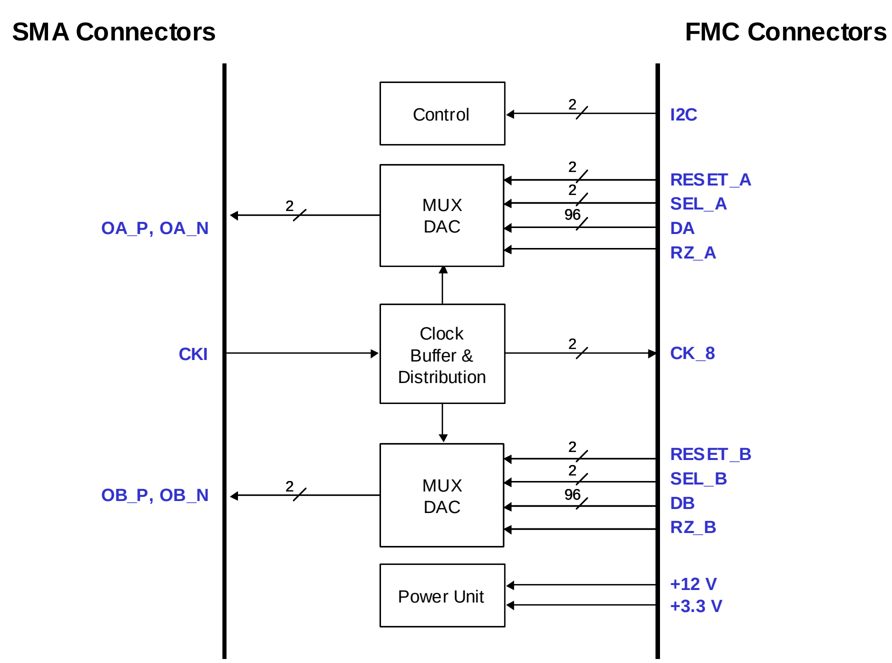
PRODUCT DESCRIPTION

The FMC2653 module is equipped with two Euvis MD653D digital-to-analog converters (DAC's). At 4 GSPS, the module provides analog outputs with bandwidth from DC to 2 GHz (Nyquist bandwidth). It can be selected to operate in return-to-zero mode to extend the usable bandwidth to 2 ~ 4 GHz. The 96 LVDS pairs of digital data are fed through two FMC connectors, a high-pin-count (HPC) and a low-pin-count (LPC) connector. The digital data multiplexing ratio is 4:1 and the digital data rate is 1 GBPS with the DAC's operating at 4 GSPS. Sampling window select (SEL's), Return-to-Zero select, and reset signals of the two DAC's can be independently controlled via the FMC connectors. The module includes two clock buffers to relax the need of high-power clock source. Both amplitudes and duty cycles of clock buffers can be programmed though I^2C interface or use factory preset values.

KEY FEATURES

- Dual 12-bit DAC's
- 0.5 ~ 4 GSPS sampling rate
- Selectable Return-to-Zero mode extends usable bandwidth to 2 ~ 4 GHz
- On-board clock buffers with adjustable gain and duty cycle
- Power supplies needed from carrier: 12V and 3.3 V
- Compliant with Vita 57.1 standard

BLOCK DIAGRAM



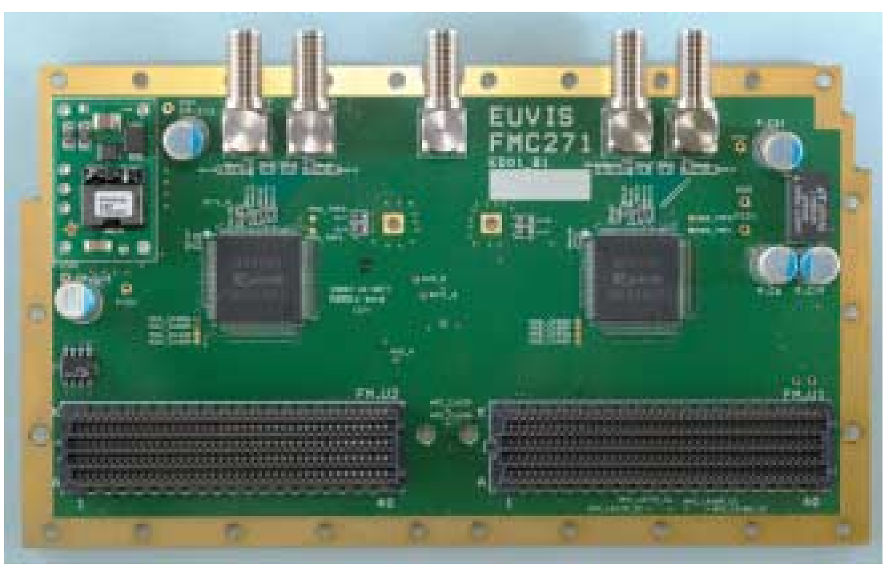
ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min	Typical	Max	Unit
Operating Temperature	T_o		25		°C
Sampling Rate	f_{data}	0.5	4	4	GSPS
Clock Frequency	f_{CK}	0.5	4	4	GHz
Clock Input Power	P_{CK}	+3	+6	+10	dBm
Output Frequency[1]	f_{out}	0		2	GHz
Output Level[2]	V_{out}	-635		0	mV
Output Power	P_{out}	-4		0	dBm
Output Residue Phase Noise[3]	N_{φ}			-130	dBC/Hz
Output Port Return Loss	RL_{RF}		15		dB
Power Supply	V_{33}		+3.3		V
	I_{33}		150		mA
	V_{120}		+12		V
	I_{120}		0.8		A

[1]Normal operation has usable bandwidth from DC to Nyquist bandwidth, 2 GHz, at 4 GSPS. In return-to-zero(RZ) mode, the usable bandwidth can be DC ~ 2 GHz and 2 ~ 4 GHz.
[2]If external 50-ohm loads are terminated to ground, the analog outputs will have voltage swings from ground to – 0.6 V with a common mode voltage of –0.3 V. If a positive analog output common mode level is desired, the external 50 ohm loads can be terminated to a positive voltage Vpull with a resultant analog output common mode voltage of (Vpull – 0.6)/2. Vpull should not exceed 5 V.
[3]10 KHz offset

TERMINAL DESCRIPTION

Name	Function	I/O	Signal
CKI	Input Clock	I	RF
OAP	CH A Analog Output Positive	O	RF
OAN	CH A Analog Output Negative	O	RF
OBP	CH B Analog Output Positive	O	RF
OBN	CH B Analog Output Negative	O	RF
GND	Ground		DC
DA	48 LVDS Pairs of Digital Data Inputs for CH A	I	RF
DB	48 LVDS Pairs of Digital Data Inputs for CH B	I	RF
RESET_A	LVDS Pair inputs for CH A DAC Reset	I	RF
RESET_B	LVDS Pair inputs for CH B DAC Reset	I	RF
SEL_A	CH A DAC Sampling Window Select	I	DC
SEL_B	CH B DAC Sampling Window Select	I	DC
RZ_A	CH A DAC Return-to-Zero Mode Select	I	DC
RZ_B	CH B DAC Return-to-Zero Mode Select	I	DC
SCK	I2C Clock	I	RF
SDA	I2C Data	I/O	RF



SWITCHING CHARACTERISTICS

Parameter	Description	Min	Typ	Max	Units
Data, Reset, CK_8: LVDS Logic					
V_{IH}	Input Voltage High		1.4		V
V_{IL}	Input Voltage Low		1		V
I	Input driving current		2		mA
T_s	Setup time	0.2			ns
T_h	Hold time	0.2			ns
SEL and RZ: LVCOMS25 Logic					
V_{IH}	Input Voltage High	1.7	2.5	2.8	V
V_{IL}	Input Voltage Low	-0.3	0	0.7	V
I	Input driving current		250		uA
I2C SDA, SCK: LVTTL33 Logic					
Speed	Standard		100		KHz
	Fast		400		KHz
	High-Speed		3400		KHz
V_{IH}	Input Voltage High	2	3.3		V
V_{IL}	Input Voltage Low		0	1	V
I	Input driving current			±1	uA
C_{in}	Input Capacitance			2	pF
V_{Hys}	Input Hysteresis	0.3			V

PIN ASSIGNMENT

Signal Name	FMC Pin Name	
MDA_RESETP	LPC_LA06P	P2.C10
MDA_RESETN	LPC_LA06N	P2.C11
MDA_SEL1	LPC_LA01P	P2.D8
MDA_SEL2	LPC_LA01N	P2.D9
MDA_RZ_SEL	HPC_HA01P	P1.E2
MDB_RESETP	HPC_HA02P	P1.K7
MDB_RESETN	HPC_HA02N	P1.K8
MDB_SEL1	HPC_HA03P	P1.J6
MDB_SEL2	HPC_HA03N	P1.J7
MDB_RZ_SEL	HPC_HA01N	P1.E3
CKD8FP	HPC_CLK00P	P1.H4
CKD8FN	HPC_CLK00N	P1.H5
+12V	12P0V	P1.C35
	12P0V	P1.C37
	12P0V	P2.C35
	12P0V	P2.C37
+3.3V	3P3V	P1.C39
	3P3VAUX	P1.D32
	3P3V	P1.D36
	3P3V	P1.D38
	3P3V	P1.D40
	3P3V	P2.C39
	3P3VAUX	P2.D32
	3P3V	P2.D36
	3P3V	P2.D38
	3P3V	P2.D40

MUXDAC A Data	FMC Pin	
A11	LPC_LA32P	P2.H37
	LPC_LA32N	P2.H38
B11	LPC_LA33P	P2.G36
	LPC_LA33N	P2.G37
C11	LPC_LA30P	P2.H34
	LPC_LA30N	P2.H35
D11	LPC_LA31P	P2.G33
	LPC_LA31N	P2.G34
A10	LPC_LA28P	P2.H31
	LPC_LA28N	P2.H32
B10	LPC_LA29P	P2.G30
	LPC_LA29N	P2.G31
C10	LPC_LA24P	P2.H28
	LPC_LA24N	P2.H29
D10	LPC_LA25P	P2.G27
	LPC_LA25N	P2.G28
A9	LPC_LA18P	P2.C22
	LPC_LA18N	P2.C23
B9	LPC_LA23P	P2.D23
	LPC_LA23N	P2.D24
C9	LPC_LA21P	P2.H25
	LPC_LA21N	P2.H26
D9	LPC_LA22P	P2.G24
	LPC_LA22N	P2.G25
A8	LPC_LA26P	P2.D26
	LPC_LA26N	P2.D27
B8	LPC_LA27P	P2.C26
	LPC_LA27N	P2.C27
C8	LPC_LA19P	P2.H22
	LPC_LA19N	P2.H23
D8	LPC_LA20P	P2.G21
	LPC_LA20N	P2.G22

MUXDAC A Data	FMC Pin	
A7	LPC_LA17P	P2.D20
	LPC_LA17N	P2.D21
B7	LPC_LA14P	P2.C18
	LPC_LA14N	P2.C19
C7	LPC_LA13P	P2.D17
	LPC_LA13N	P2.D18
D7	LPC_LA15P	P2.H19
	LPC_LA15N	P2.H20
A6	LPC_LA16P	P2.G18
	LPC_LA16N	P2.G19
B6	LPC_LA11P	P2.H16
	LPC_LA11N	P2.H17
C6	LPC_LA12P	P2.G15
	LPC_LA12N	P2.G16
D6	LPC_LA09P	P2.D14
	LPC_LA09N	P2.D15
A5	LPC_LA10P	P2.C14
	LPC_LA10N	P2.C15
B5	LPC_LA07P	P2.H13
	LPC_LA07N	P2.H14
C5	LPC_LA08P	P2.G12
	LPC_LA08N	P2.G13
D5	LPC_LA05P	P2.D11
	LPC_LA05N	P2.D12
A4	LPC_LA04P	P2.H10
	LPC_LA04N	P2.H11
B4	LPC_LA03P	P2.G9
	LPC_LA03N	P2.G10
C4	LPC_LA02P	P2.H7
	LPC_LA02N	P2.H8
D4	LPC_LA00P	P2.G6
	LPC_LA00N	P2.G7

MUXDAC A Data	FMC Pin	
A3	HPC_LA06P	P1.C10
	HPC_LA06N	P1.C11
B3	HPC_LA01P	P1.D8
	HPC_LA01N	P1.D9
C3	HPC_LA00P	P1.G6
	HPC_LA00N	P1.G7
D3	HPC_LA05P	P1.D11
	HPC_LA05N	P1.D12
A2	HPC_LA03P	P1.G9
	HPC_LA03N	P1.G10
B2	HPC_LA04P	P1.H10
	HPC_LA04N	P1.H11
C2	HPC_LA08P	P1.G12
	HPC_LA08N	P1.G13
D2	HPC_LA07P	P1.H13
	HPC_LA07N	P1.H14
A1	HPC_HA05P	P1.E6
	HPC_HA05N	P1.E7
B1	HPC_HA04P	P1.F7
	HPC_HA04N	P1.F8
C1	HPC_HA09P	P1.E9
	HPC_HA09N	P1.E10
D1	HPC_HA08P	P1.F10
	HPC_HA08N	P1.F11
A0	HPC_HA07P	P1.J9
	HPC_HA07N	P1.J10
B0	HPC_HA06P	P1.K10
	HPC_HA06N	P1.K11
C0	HPC_HA13P	P1.E12
	HPC_HA13N	P1.E13
D0	HPC_HA12P	P1.F13
	HPC_HA12N	P1.F14

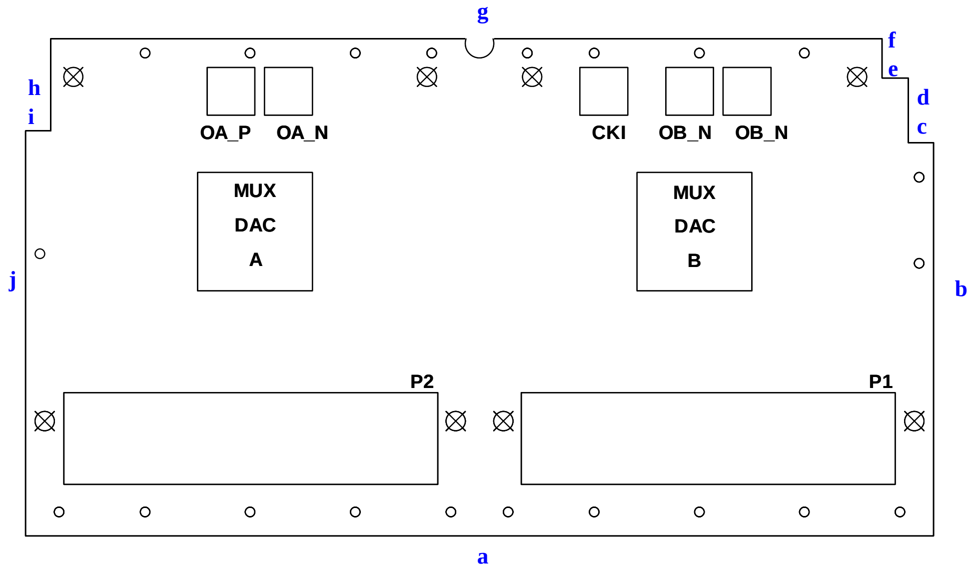
MUXDAC B Data	FMC Pin	
A11	HPC_HB17P	P1.K37
	HPC_HB17N	P1.K38
B11	HPC_HB18P	P1.J36
	HPC_HB18N	P1.J37
C11	HPC_HB16P	P1.F34
	HPC_HB16N	P1.F35
D11	HPC_HB19P	P1.E33
	HPC_HB19N	P1.E34
A10	HPC_HB14P	P1.K34
	HPC_HB14N	P1.K35
B10	HPC_HB15P	P1.J33
	HPC_HB15N	P1.J34
C10	HPC_HB12P	P1.F31
	HPC_HB12N	P1.F32
D10	HPC_HB13P	P1.E30
	HPC_HB13N	P1.E31
A9	HPC_HB10P	P1.K31
	HPC_HB10N	P1.K32
B9	HPC_HB11P	P1.J30
	HPC_HB11N	P1.J31
C9	HPC_HB08P	P1.F28
	HPC_HB08N	P1.F29
D9	HPC_HB09P	P1.E27
	HPC_HB09N	P1.E28
A8	HPC_HB06P	P1.K28
	HPC_HB06N	P1.K29
B8	HPC_HB07P	P1.J27
	HPC_HB07N	P1.J28
C8	HPC_HB00P	P1.K25
	HPC_HB00N	P1.K26
D8	HPC_HB01P	P1.J24
	HPC_HB01N	P1.J25

MUXDAC B Data	FMC Pin	
A7	HPC_LA21P	P1.H25
	HPC_LA21N	P1.H26
B7	HPC_LA22P	P1.G24
	HPC_LA22N	P1.G25
C7	HPC_LA23P	P1.D23
	HPC_LA23N	P1.D24
D7	HPC_LA17P	P1.D20
	HPC_LA17N	P1.D21
A6	HPC_HA23P	P1.K22
	HPC_HA23N	P1.K23
B6	HPC_HA22P	P1.J21
	HPC_HA22N	P1.J22
C6	HPC_HA19P	P1.F19
	HPC_HA19N	P1.F20
D6	HPC_HA20P	P1.E18
	HPC_HA20N	P1.E19
A5	HPC_HA21P	P1.K19
	HPC_HA21N	P1.K20
B5	HPC_HA18P	P1.J18
	HPC_HA18N	P1.J19
C5	HPC_HA17P	P1.K16
	HPC_HA17N	P1.K17
D5	HPC_HA15P	P1.F16
	HPC_HA15N	P1.F17
A4	HPC_HA14P	P1.J15
	HPC_HA14N	P1.J16
B4	HPC_HA11P	P1.J12
	HPC_HA11N	P1.J13
C4	HPC_HA10P	P1.K13
	HPC_HA10N	P1.K14
D4	HPC_HA16P	P1.E15
	HPC_HA16N	P1.E16

MUXDAC B Data	FMC Pin	
A3	HPC_LA15P	P1.H19
	HPC_LA15N	P1.H20
B3	HPC_LA16P	P1.G18
	HPC_LA16N	P1.G19
C3	HPC_LA14P	P1.C18
	HPC_LA14N	P1.C19
D3	HPC_LA13P	P1.D17
	HPC_LA13N	P1.D18
A2	HPC_LA11P	P1.H16
	HPC_LA11N	P1.H17
B2	HPC_LA12P	P1.G15
	HPC_LA12N	P1.G16
C2	HPC_LA09P	P1.D14
	HPC_LA09N	P1.D15
D2	HPC_LA10P	P1.C14
	HPC_LA10N	P1.C15
A1	HPC_LA25P	P1.G27
	HPC_LA25N	P1.G28
B1	HPC_LA24P	P1.H28
	HPC_LA24N	P1.H29
C1	HPC_LA29P	P1.G30
	HPC_LA29N	P1.G31
D1	HPC_LA28P	P1.H31
	HPC_LA28N	P1.H32
A0	HPC_LA31P	P1.G33
	HPC_LA31N	P1.G34
B0	HPC_LA30P	P1.H34
	HPC_LA30N	P1.H35
C0	HPC_LA33P	P1.G36
	HPC_LA33N	P1.G37
D0	HPC_LA32P	P1.H37
	HPC_LA32N	P1.H38

BOARD OUTLINE AND DIMENSIONS:

TOP VIEW



All dimensions use the bottom left corner of the board as the origin. All dimensions are in millimeters (mm). Board thickness is 1.62 mm.

Board Edge Lengths

Edge	Length	Edge	Length	Edge	Length
a	139	b	61.7	c	2.4
d	9.1	e	2.1	f	8
g	131.3	h	21.9	i	3
j	56.9	Width	139	Height	78.8

⊠ ***FMC Connector Mount Hole Locations (x, y)***

73, 18.4	136, 18.4	3, 18.4	66, 18.4

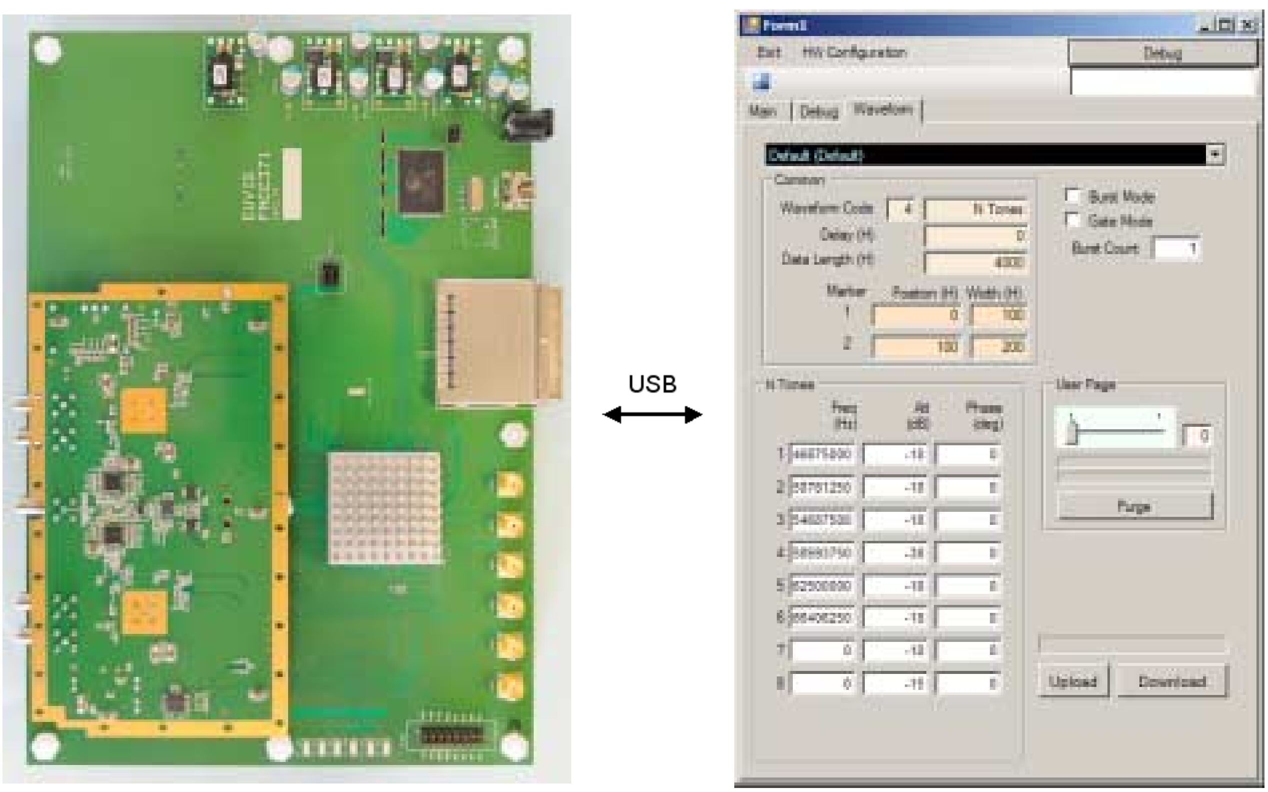
SMA Locations (x, y)

CKI	68.3, 68		
OA_P	37.0, 68	OB_P	98.8, 68
OA_N	47.4, 68	OB_N	109.2, 68

TEST SETUP

In applications, FMC2653 requires a VITA 57.1-compliant carrier board to provide all digital data, DAC controls, I^2C signal, and DC powers via FMC connectors. The carrier must provide two power supplies, +12V and +3.3V, with minimum current capacities of 1A and 500mA respectively. Digital data and DAC resets are in LVDS pairs. The DAC timing selects and return-to-zero mode select are single-ended LVCMOS25. The carrier board can be an advanced FPGA evaluation board, such as Xilinx VC707, with proper configurations.

The FMC module is tested using Euvis carrier FMCC371 as shown in following figure. The carrier consists of a Xilinx XC6VLX130T, a USB controller, and power modules. In the test setup, the carrier is controlled by a PC host via the USB interface. The carrier can store up to 2 x 512 K words of data in memory. The maximum data length is 64us at 4 GSPS for each channel. Several built-in waveforms are available as in our AWG's GUI. Waveform generation and download are performed in GUI.



Euvis Inc.

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