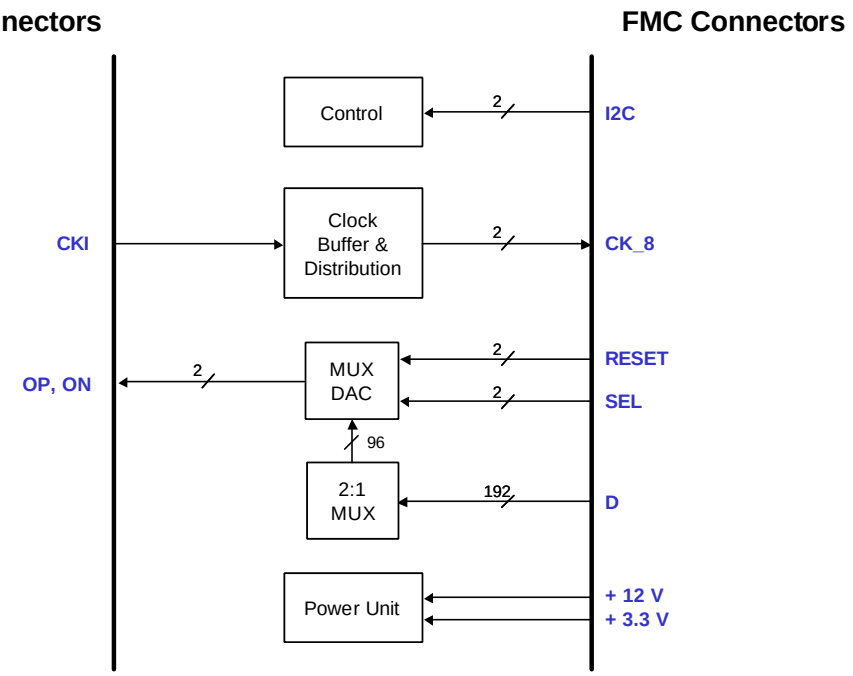
FMC201 – 8-GSPS 12-bit DAC with 2:1 MUX's FMC Module

PRODUCT DESCRIPTION

The ***FMC201*** module is equipped with the ***Euvis*** **MD662H** digital-to-analog converter (DAC). At 8 GSPS, the module provides analog outputs with bandwidth from DC to 4 GHz (Nyquist bandwidth). In addition to the 4:1 internal multiplexer of the **MD662H**, the module includes four 2:1 high-speed ***Euvis*** **MX2412H** multiplexers to further lower the input data rate and can directly accept advanced FPGA LVDS outputs. The total multiplexing ratio is 8:1 and the digital data rate is 1 Gb/s for the DAC operated at 8 GSPS. The 96 LVDS pairs of digital data are fed through two FMC connectors, a high-pin-count (HPC) and a low-pin-count (LPC) connector. Sampling window select (SEL's) and reset signals of the DAC can be independently controlled via the FMC connectors. The module includes three clock buffers to relax the need of high-power clock source. The amplitudes and duty cycles of the clock buffers can be programmed though the I^2C interface.

KEY FEATURES

- 12-bit DAC
- 1 ~ 8 GSPS sampling rate
- On-board clock buffers with adjustable gain and duty cycle
- Power supplies needed from carrier: 12V and 3.3 V
- Compliant with Vita 57.1 standard



ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min	Typical	Max	Unit
Operating Temperature	T_o		25		^oC
Sampling Rate	f_{data}	1	8	8	GSPS
Clock Frequency	f_{CK}	0.5	4	4	GHz
Clock Input Power	P_{CK}	+3	+6	+10	dBm
Output Frequency	f_{out}	0		4	GHz
Output Level[1]	V_{out}	-635		0	mV
Output Power	P_{out}	-4		0	dBm
Output Residue Phase Noise[2]	N_f			-130	dBC/Hz
Output Port Return Loss	RL_{RF}		15		dB
Power Supply	V_{33}		+3.3		V
	I_{33}		300		mA
	V_{120}		+12		V
	I_{120}		800		mA

[1]If external 50 ohm loads are terminated to ground, the analog outputs will have voltage swings from ground to – 0.6 V with a common mode voltage of –0.3 V. If a positive analog output common mode level is desired, the external 50 ohm loads can be terminated to a positive voltage Vpull with a resultant analog output common mode voltage of (Vpull – 0.6)/2. Vpull should not exceed 5 V.

[2]10 KHz offset

TERMINAL DESCRIPTION

Name	Function	I/O	Signal
CKI	Input Clock	I	RF
OP	Analog Output Positive	O	RF
ON	Analog Output Negative	O	RF
GND	Ground		DC
D	96 LVDS Pairs of Digital Data Inputs	I	RF
RESET_A	LVDS Pair inputs for DAC Reset	I	RF
SEL_A	DAC Sampling Window Select	I	DC
SCK	I2C Clock	I	RF
SDA	I2C Data	I/O	RF

SWITCHING CHARACTERISTICS

Parameter	Description	Min	Typ	Max	Units
Data, Reset, CK_8: LVDS Logic					
V_{IH}	Input Voltage High		1.4		V
V_{IL}	Input Voltage Low		1		V
I	Input driving current		2		mA
T_s	Setup time	0.2			ns
T_h	Hold time	0.2			ns
SEL and RZ: LVCOMS25 / LVCMOS18 Logic					
V_{IH}	Input Voltage High	1.5	2.5	2.8	V
V_{IL}	Input Voltage Low	-0.3	0	0.5	V
I	Input driving current		250		uA
I2C SDA, SCK: LVTTL33 Logic					
Speed	Standard		100		KHz
	Fast		400		KHz
	High-Speed		3400		KHz
V_{IH}	Input Voltage High	2	3.3		V
V_{IL}	Input Voltage Low		0	1	V
I	Input driving current			±1	uA
C_{in}	Input Capacitance			2	pF
V_{Hys}	Input Hysteresis	0.3			V

PIN ASSIGNMENT

Signal Name	FMC Pin Name	
MDA_RESETP	LPC_LA18P	P2.C22
MDA_RESETN	LPC_LA18N	P2.C23
MDA_SEL1	LPC_LA14P	P2.C18
MDA_SEL2	LPC_LA14N	P2.C19
MXA_SEL1	HPC_HB19N	P1.E33
MXB_SEL1	HPC_HB19P	P1.E34
MXC_SEL1	LPC_LA02N	P2.H7
MXD_SEL1	LPC_LA02P	P2.H8
MUX_CK_OE	LPC_LA13P	P2.D17
MUX_CK_POL	LPC_LA13N	P2.D18
CKD8FP	HPC_CLK00P	P1.H4
CKD8FN	HPC_CLK00N	P1.H5
I2C SCL	HPC_SCL	P1.C30
I2C SDA	HPC_SDA	P1.C31
+12V	12P0V	P1.C35
	12P0V	P1.C37
	12P0V	P2.C35
	12P0V	P2.C37
+3.3V	3P3V	P1.C39
	3P3VAUX	P1.D32
	3P3V	P1.D36
	3P3V	P1.D38
	3P3V	P1.D40
	3P3V	P2.C39
	3P3VAUX	P2.D32
	3P3V	P2.D36
	3P3V	P2.D38
	3P3V	P2.D40

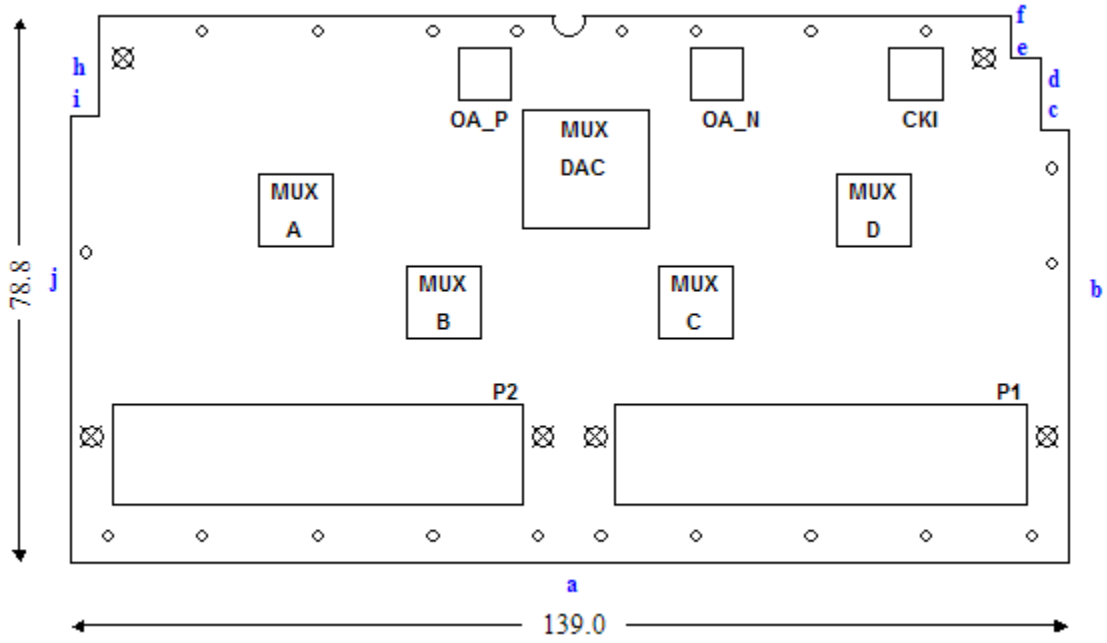
MUXDAC Data		FMC Pin	
A11	A	HPC_HB17P	P1.K37
		HPC_HB17N	P1.K38
	B	HPC_HB18P	P1.J36
		HPC_HB18N	P1.J37
B11	A	HPC_HB14P	P1.K34
		HPC_HB14N	P1.K35
	B	HPC_HB15P	P1.J33
		HPC_HB15N	P1.J34
C11	A	HPC_HB16P	P1.F34
		HPC_HB16N	P1.F35
	B	HPC_HB12P	P1.F31
		HPC_HB12N	P1.F32
D11	A	HPC_HB11P	P1.J30
		HPC_HB11N	P1.J31
	B	HPC_HB10P	P1.K31
		HPC_HB10N	P1.K32
A10	A	HPC_HB08P	P1.F28
		HPC_HB08N	P1.F29
	B	HPC_HB07P	P1.J27
		HPC_HB07N	P1.J28
B10	A	HPC_HB04P	P1.F25
		HPC_HB04N	P1.F26
	B	HPC_HB06P	P1.K28
		HPC_HB06N	P1.K29
C10	A	HPC_HB00P	P1.K25
		HPC_HB00N	P1.K26
	B	HPC_HB02P	P1.F22
		HPC_HB02N	P1.F23
D10	A	HPC_HB01P	P1.J24
		HPC_HB01N	P1.J25
	B	HPC_HB03P	P1.E21
		HPC_HB03N	P1.E22
A9	A	HPC_LA25P	P1.G27
		HPC_LA25N	P1.G28
	B	HPC_LA24P	P1.H28
		HPC_LA24N	P1.H29
B9	A	HPC_LA29P	P1.G30
		HPC_LA29N	P1.G31
	B	HPC_LA28P	P1.H31
		HPC_LA28N	P1.H32
C9	A	HPC_LA31P	P1.G33
		HPC_LA31N	P1.G34
	B	HPC_LA30P	P1.H34
		HPC_LA30N	P1.H35
D9	A	HPC_LA33P	P1.G36
		HPC_LA33N	P1.G37
	B	HPC_LA32P	P1.H37
		HPC_LA32N	P1.H38
A8	A	HPC_LA26P	P1.D26
		HPC_LA26N	P1.D27
	B	HPC_LA21P	P1.H25
		HPC_LA21N	P1.H26
B8	A	HPC_LA27P	P1.C26
		HPC_LA27N	P1.C27
	B	HPC_LA22P	P1.G24
		HPC_LA22N	P1.G25
C8	A	HPC_LA23P	P1.D23
		HPC_LA23N	P1.D24
	B	HPC_LA19P	P1.H22
		HPC_LA19N	P1.H23
D8	A	HPC_LA20P	P1.G21
		HPC_LA20N	P1.G22
	B	HPC_LA17P	P1.D20
		HPC_LA17N	P1.D21

MUXDAC Data		FMC Pin	
A7	A	HPC_HA12P	P1.F13
		HPC_HA12N	P1.F14
	B	HPC_HA13P	P1.E12
		HPC_HA13N	P1.E13
B7	A	HPC_HA08P	P1.F10
		HPC_HA08N	P1.F11
	B	HPC_HA09P	P1.E9
		HPC_HA09N	P1.E10
C7	A	HPC_HA04P	P1.F7
		HPC_HA04N	P1.F8
	B	HPC_HA05P	P1.E6
		HPC_HA05N	P1.E7
D7	A	HPC_HA00P	P1.F4
		HPC_HA00N	P1.F5
	B	HPC_HA01P	P1.E2
		HPC_HA01N	P1.E3
A6	A	HPC_HA16P	P1.E15
		HPC_HA16N	P1.E16
	B	HPC_HA15P	P1.F16
		HPC_HA15N	P1.F17
B6	A	HPC_HA18P	P1.J18
		HPC_HA18N	P1.J19
	B	HPC_HA20P	P1.E18
		HPC_HA20N	P1.E19
C6	A	HPC_HA21P	P1.K19
		HPC_HA21N	P1.K20
	B	HPC_HA19P	P1.F19
		HPC_HA19N	P1.F20
D6	A	HPC_HA22P	P1.J21
		HPC_HA22N	P1.J22
	B	HPC_HA23P	P1.K22
		HPC_HA23N	P1.K23
A5	A	HPC_HA17P	P1.K16
		HPC_HA17N	P1.K17
	B	HPC_HA14P	P1.J15
		HPC_HA14N	P1.J16
B5	A	HPC_HA10P	P1.K13
		HPC_HA10N	P1.K14
	B	HPC_HA11P	P1.J12
		HPC_HA11N	P1.J13
C5	A	HPC_HA06P	P1.K10
		HPC_HA06N	P1.K11
	B	HPC_HA07P	P1.J9
		HPC_HA07N	P1.J10
D5	A	HPC_HA02P	P1.K7
		HPC_HA02N	P1.K8
	B	HPC_HA03P	P1.J6
		HPC_HA03N	P1.J7
A4	A	HPC_LA02P	P1.H7
		HPC_LA02N	P1.H8
	B	HPC_LA00P	P1.G6
		HPC_LA00N	P1.G7
B4	A	HPC_LA13P	P1.D17
		HPC_LA13N	P1.D18
	B	HPC_LA09P	P1.D14
		HPC_LA09N	P1.D15
C4	A	HPC_LA05P	P1.D11
		HPC_LA05N	P1.D12
	B	HPC_LA06P	P1.C10
		HPC_LA06N	P1.C11
D4	A	HPC_LA10P	P1.C14
		HPC_LA10N	P1.C15
	B	HPC_LA14P	P1.C18
		HPC_LA14N	P1.C19

MUXDAC Data		FMC Pin	
A3	A	HPC_LA03P	P1.G9
		HPC_LA03N	P1.G10
	B	HPC_LA04P	P1.H10
		HPC_LA04N	P1.H11
B3	A	HPC_LA08P	P1.G12
		HPC_LA08N	P1.G13
	B	HPC_LA07P	P1.H13
		HPC_LA07N	P1.H14
C3	A	HPC_LA12P	P1.G15
		HPC_LA12N	P1.G16
	B	HPC_LA11P	P1.H16
		HPC_LA11N	P1.H17
D3	A	HPC_LA16P	P1.G18
		HPC_LA16N	P1.G19
	B	HPC_LA15P	P1.H19
		HPC_LA15N	P1.H20
A2	A	LPC_LA32P	P2.H37
		LPC_LA32N	P2.H38
	B	LPC_LA33P	P2.G36
		LPC_LA33N	P2.G37
B2	A	LPC_LA30P	P2.H34
		LPC_LA30N	P2.H35
	B	LPC_LA31P	P2.G33
		LPC_LA31N	P2.G34
C2	A	LPC_LA28P	P2.H31
		LPC_LA28N	P2.H32
	B	LPC_LA29P	P2.G30
		LPC_LA29N	P2.G31
D2	A	LPC_LA24P	P2.H28
		LPC_LA24N	P2.H29
	B	LPC_LA25P	P2.G27
		LPC_LA25N	P2.G28
A1	A	LPC_LA27P	P2.C26
		LPC_LA27N	P2.C27
	B	LPC_LA26P	P2.D26
		LPC_LA26N	P2.D27
B1	A	LPC_LA21P	P2.H25
		LPC_LA21N	P2.H26
	B	LPC_LA22P	P2.G24
		LPC_LA22N	P2.G25
C1	A	LPC_LA23P	P2.D23
		LPC_LA23N	P2.D24
	B	LPC_LA19P	P2.H22
		LPC_LA19N	P2.H23
D1	A	LPC_LA20P	P2.G21
		LPC_LA20N	P2.G22
	B	LPC_LA17P	P2.D20
		LPC_LA17N	P2.D21
A0	A	LPC_LA15P	P2.H19
		LPC_LA15N	P2.H20
	B	LPC_LA16P	P2.G18
		LPC_LA16N	P2.G19
B0	A	LPC_LA11P	P2.H16
		LPC_LA11N	P2.H17
	B	LPC_LA12P	P2.G15
		LPC_LA12N	P2.G16
C0	A	LPC_LA07P	P2.H13
		LPC_LA07N	P2.H14
	B	LPC_LA08P	P2.G12
		LPC_LA08N	P2.G13
D0	A	LPC_LA04P	P2.H10
		LPC_LA04N	P2.H11
	B	LPC_LA03P	P2.G9
		LPC_LA03N	P2.G10

BOARD OUTLINE AND DIMENSIONS:

TOP VIEW



P1 is the primary HPC connector and P2 is the LPC connector. All dimensions use the bottom left corner of the board as the origin. All dimensions are in millimeters (mm). Board thickness is 1.62 mm.

Board Edge Lengths

Edge	Length	Edge	Length	Edge	Length
a	139	**b**	61.7	**c**	2.4
d	9.1	**e**	2.1	**f**	8
g	131.3	**h**	21.9	**i**	3
j	56.9	Width	139	Height	78.8

⊠ ***FMC Connector Mount Hole Locations (x, y)***

73, 18.4	136, 18.4	3, 18.4	66, 18.4

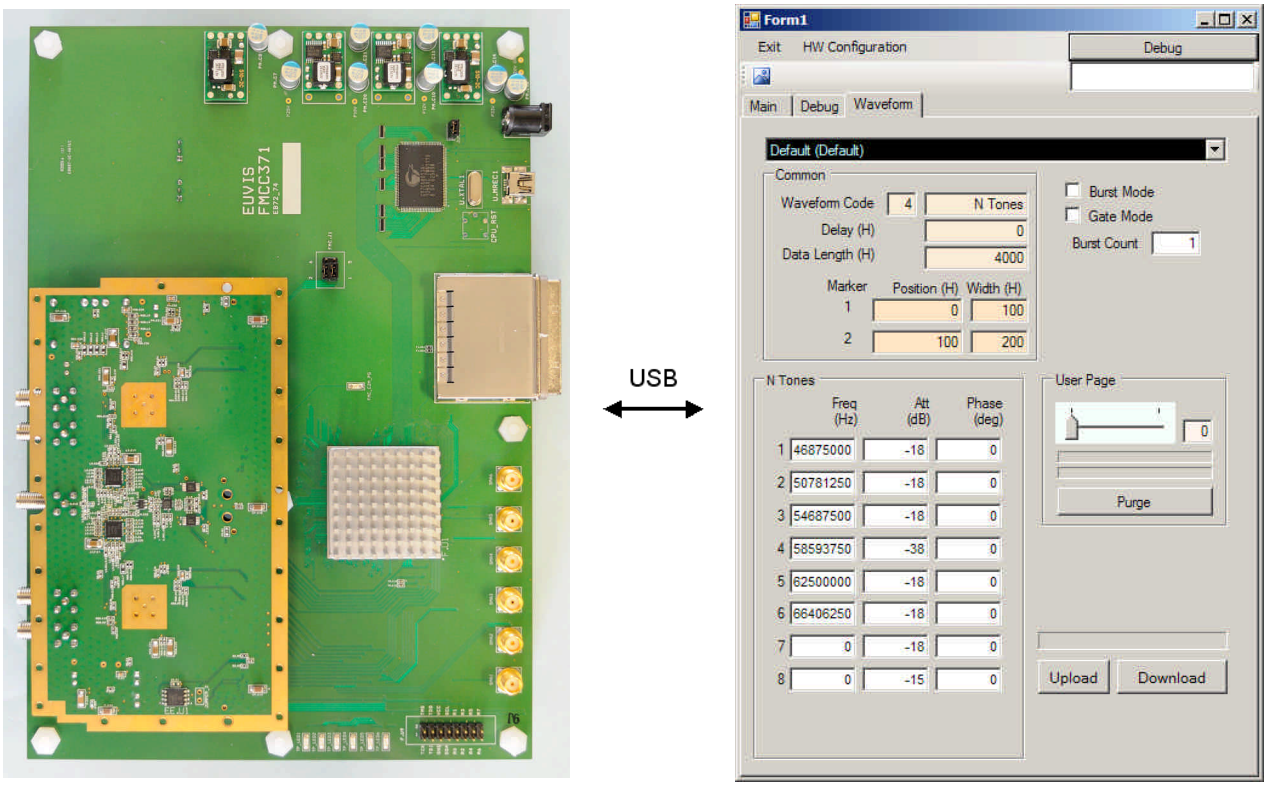
SMA Locations (x, y)

CKI	118.6, 69.3
OA_P	61.7, 69.3
OA_N	92.1, 69.3

TEST SETUP

In applications, FMC201 requires a VITA 57.1-compliant carrier board to provide all digital data, DAC controls, I^2C signal, and DC powers via FMC connectors. The carrier must provide two power supplies, +12V and +3.3V, with minimum current capacities of 1A and 500mA respectively. Digital data and DAC resets are in LVDS pairs. The DAC timing selects are single-ended LVCMOS25. The carrier board can be an advanced FPGA evaluation board, such as Xilinx VC707, with proper configurations.

The FMC module is tested using Euvis carrier FMCC371 as shown in following figure. The carrier consists of a Xilinx XC6VLX130T, a USB controller, and power modules. In the test setup, the carrier is controlled by a PC host via the USB interface. The carrier can store up to 2 x 512 K words of data in memory. The maximum data length is 64us at 4 GSPS for each channel. Several built-in waveforms are available as in our AWG's GUI. Waveform generation and download are performed in GUI.



Euvis Inc.

Ordering Information:

Email to: Sales@euvis.com
Or call: (805) 583-9888 x108 Sales Department
Or fax: (805) 583-9889

The information contained in this document is based on preliminary measured results. Characteristic data and other specifications are subject to change without notice. Customers are advised to confirm information in this advanced datasheet prior to using this information or placing the order.

Euvis Inc. does not assume any liability arising from the application or use of any product or circuit described herein, neither does it convey any license under its patents or any other rights.