

## **FMC1657 – 5-GSPS 12-bit Single DAC FMC Module**

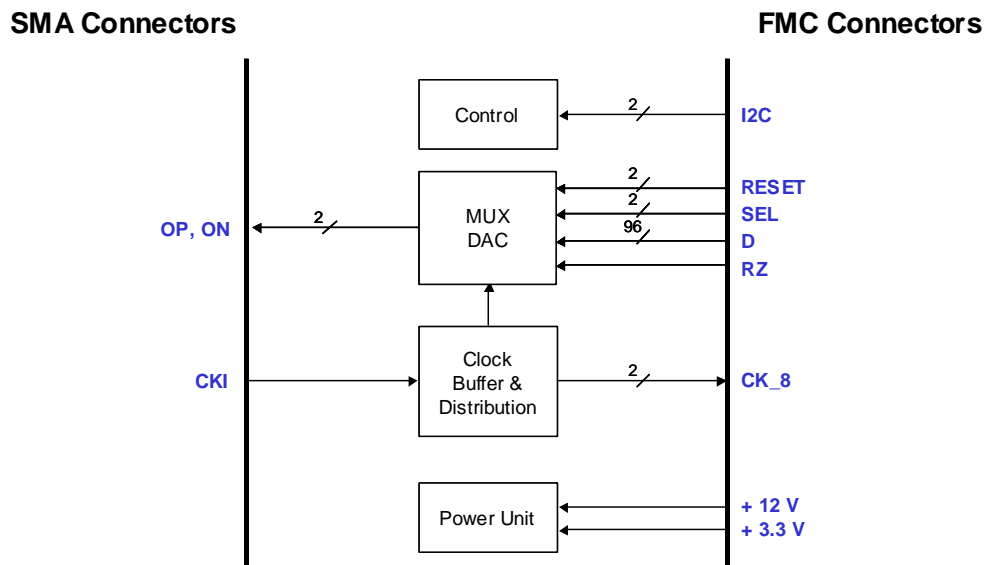
### **PRODUCT DESCRIPTION**

The **FMC1657** module is equipped with an **Euvis MD657B** digital-to-analog converters (DAC's). At 5 GSPS, the module provides analog outputs with bandwidth from DC to 2.5 GHz (Nyquist bandwidth). It can be selected to operate in return-to-zero mode to extend the usable bandwidth to 2.5 ~ 5 GHz. The 48 LVDS pairs of digital data are fed through a FMC connector, a high-pin-count (HPC) connector. The digital data multiplexing ratio is 4:1 and the digital data rate is 1.25 GBPS with the DAC's operating at 5 GSPS. Sampling window select (SEL's), Return-to-Zero select, and reset signals of the DAC's can be independently controlled via the FMC connector. The module includes a clock buffer to relax the need of high-power clock source. Both amplitude and duty cycle of the clock buffer can be programmed though I<sup>2</sup>C interface or use factory preset values.

### **KEY FEATURES**

- 12-bit DAC's
- 1 ~ 5 GSPS sampling rate
- Selectable Return-to-Zero mode extends usable bandwidth to 2.5 ~ 5 GHz
- On-board clock buffers with adjustable gain and duty cycle
- Power supplies needed from carrier: 12V and 3.3 V
- Compliant with Vita 57.1 standard

### **BLOCK DIAGRAM**



**ELECTRICAL SPECIFICATIONS**

Parameter	Symbol	Min	Typical	Max	Unit
Operating Temperature	$T_o$		25		°C
Sampling Rate	$f_{data}$	1	5	5	GSPS
Clock Frequency	$f_{CK}$	1	5	5	GHz
Clock Input Power	$P_{CK}$	+3	+6	+10	dBm
Output Frequency <sup>1</sup>	$f_{out}$	0		2.5	GHz
Output Level <sup>2</sup>	$V_{out}$	-635		0	mV
Output Power	$P_{out}$	-4		0	dBm
Output Residue Phase Noise <sup>3</sup>	$N_\phi$			-130	dBc/Hz
Output Port Return Loss	$RL_{RF}$		15		dB
Power Supply	$V_{33}$		+3.3		V
	$I_{33}$		100		mA
	$V_{120}$		+12		V
	$I_{120}$		0.6		A

<sup>1</sup>Normal operation has usable bandwidth from DC to Nyquist bandwidth, 2.5 GHz, at 5 GSPS.

In return-to-zero(RZ) mode, the usable bandwidth can be DC ~ 2.5 GHz and 2.5 ~ 5 GHz.

<sup>2</sup>If external 50-ohm loads are terminated to ground, the analog outputs will have voltage swings from ground to – 0.6 V with a common mode voltage of –0.3 V. If a positive analog output common mode level is desired, the external 50 ohm loads can be terminated to a positive voltage  $V_{pull}$  with a resultant analog output common mode voltage of  $(V_{pull} - 0.6)/2$ .

$V_{pull}$  should not exceed 5 V.

<sup>3</sup>10 KHz offset

**TERMINAL DESCRIPTION**

Name	Function	I/O	Signal
CKI	Input Clock	I	RF
OP	Analog Output Positive	O	RF
ON	Analog Output Negative	O	RF
GND	Ground		DC
D	48 LVDS Pairs of Digital Data Inputs	I	RF
RESET	LVDS Pair inputs for DAC Reset	I	RF
SEL	DAC Sampling Window Select	I	DC
RZ	DAC Return-to-Zero Mode Select	I	DC
SCK	I2C Clock	I	RF
SDA	I2C Data	I/O	RF

**SWITCHING CHARACTERISTICS**

Parameter	Description	Min	Typ	Max	Units
<b>Data, Reset, CK_8: LVDS Logic</b>					
V <sub>IH</sub>	Input Voltage High		1.4		V
V <sub>IL</sub>	Input Voltage Low		1		V
I	Input driving current		2		mA
T <sub>s</sub>	Setup time	0.2			ns
T <sub>h</sub>	Hold time	0.2			ns
<b>SEL and RZ: LVCOMS25 Logic</b>					
V <sub>IH</sub>	Input Voltage High	1.7	2.5	2.8	V
V <sub>IL</sub>	Input Voltage Low	-0.3	0	0.7	V
I	Input driving current		250		uA
<b>I2C SDA, SCK: LVTTTL33 Logic</b>					
Speed	Standard		100		KHz
	Fast		400		KHz
	High-Speed		3400		KHz
V <sub>IH</sub>	Input Voltage High	2	3.3		V
V <sub>IL</sub>	Input Voltage Low		0	1	V
I	Input driving current			±1	uA
C <sub>in</sub>	Input Capacitance			2	pF
V <sub>Hys</sub>	Input Hysteresis	0.3			V

**PIN ASSIGNMENT**

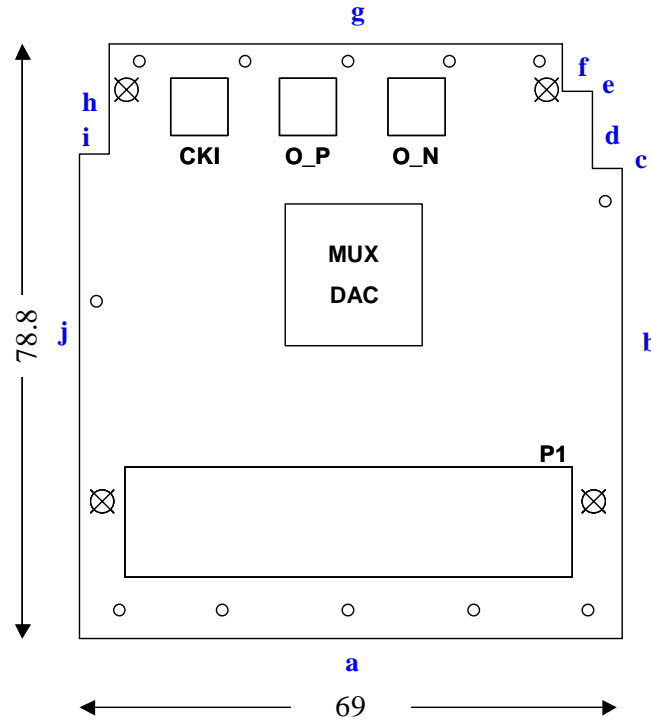
<b>Signal Name</b>	<b>FMC Pin Name</b>		<b>ML605 Bank</b>
MDA_RESETP	HPC_LA19P	P1.H22	23
MDA_RESETN	HPC_LA19N	P1.H23	23
MDA_SEL1	HPC_LA00P	P1.G6	15
MDA_SEL2	HPC_LA00N	P1.G7	15
MDA_RZ_SEL	HPC_HB00P	P1.K25	12
CK_8	HPC_CLK00P	P1.H4	24
	HPC_CLK00N	P1.H5	24
+12V	12P0V	P1.C35	n/a
	12P0V	P1.C37	n/a
+3.3V	3P3V	P1.C39	n/a
	3P3VAUX	P1.D32	n/a
	3P3V	P1.D36	n/a
	3P3V	P1.D38	n/a
	3P3V	P1.D40	n/a

MUXDAC A Data	FMC Pin		ML605 Bank	MUXDAC A Data	FMC Pin		ML605 Bank
A11	HPC_HB18P	P1.J36	12	A7	HPC_LA24P	P1.H28	23
	HPC_HB18N	P1.J37	12		HPC_LA24N	P1.H29	23
B11	HPC_HB17P	P1.K37	12	B7	HPC_LA25P	P1.G27	23
	HPC_HB17N	P1.K38	12		HPC_LA25N	P1.G28	23
C11	HPC_HB15P	P1.J33	12	C7	HPC_LA27P	P1.C26	23
	HPC_HB15N	P1.J34	12		HPC_LA27N	P1.C27	23
D11	HPC_HB14P	P1.K34	12	D7	HPC_LA26P	P1.D26	23
	HPC_HB14N	P1.K35	12		HPC_LA26N	P1.D27	23
A10	HPC_HB16P	P1.F34	12	A6	HPC_LA21P	P1.H25	23
	HPC_HB16N	P1.F35	12		HPC_LA21N	P1.H26	23
B10	HPC_HB12P	P1.F31	12	B6	HPC_LA22P	P1.G24	23
	HPC_HB12N	P1.F32	12		HPC_LA22N	P1.G25	23
C10	HPC_HB11P	P1.J30	12	C6	HPC_LA23P	P1.D23	23
	HPC_HB11N	P1.J31	12		HPC_LA23N	P1.D24	23
D10	HPC_HB10P	P1.K31	12	D6	HPC_LA18P	P1.C22	23
	HPC_HB10N	P1.K32	12		HPC_LA18N	P1.C23	23
A9	HPC_HB08P	P1.F28	12	A5	HPC_LA14P	P1.C18	22
	HPC_HB08N	P1.F29	12		HPC_LA14N	P1.C19	22
B9	HPC_HB07P	P1.J27	12	B5	HPC_LA13P	P1.D17	22
	HPC_HB07N	P1.J28	12		HPC_LA13N	P1.D18	22
C9	HPC_HB06P	P1.K28	12	C5	HPC_LA15P	P1.H19	22
	HPC_HB06N	P1.K29	12		HPC_LA15N	P1.H20	22
D9	HPC_HB04P	P1.F25	12	D5	HPC_LA16P	P1.G18	22
	HPC_HB04N	P1.F26	12		HPC_LA16N	P1.G19	22
A8	HPC_LA33P	P1.G36	23	A4	HPC_LA11P	P1.H16	22
	HPC_LA33N	P1.G37	23		HPC_LA11N	P1.H17	22
B8	HPC_LA32P	P1.H37	23	B4	HPC_LA12P	P1.G15	22
	HPC_LA32N	P1.H38	23		HPC_LA12N	P1.G16	22
C8	HPC_LA28P	P1.H31	23	C4	HPC_LA07P	P1.H13	22
	HPC_LA28N	P1.H32	23		HPC_LA07N	P1.H14	22
D8	HPC_LA29P	P1.G30	23	D4	HPC_LA08P	P1.G12	22
	HPC_LA29N	P1.G31	23		HPC_LA08N	P1.G13	22

MUXDAC A Data	FMC Pin		ML605 Bank
A3	HPC_LA05P	P1.D11	22
	HPC_LA05N	P1.D12	22
B3	HPC_LA06P	P1.C10	22
	HPC_LA06N	P1.C11	22
C3	HPC_LA04P	P1.H10	22
	HPC_LA04N	P1.H11	22
D3	HPC_LA03P	P1.G9	22
	HPC_LA03N	P1.G10	22
A2	HPC_HA21P	P1.K19	14
	HPC_HA21N	P1.K20	14
B2	HPC_HA17P	P1.K16	14
	HPC_HA17N	P1.K17	14
C2	HPC_HA10P	P1.K13	13
	HPC_HA10N	P1.K14	13
D2	HPC_HA06P	P1.K10	13
	HPC_HA06N	P1.K11	13
A1	HPC_HA02P	P1.K7	13
	HPC_HA02N	P1.K8	13
B1	HPC_HA03P	P1.J6	13
	HPC_HA03N	P1.J7	13
C1	HPC_HA08P	P1.F10	13
	HPC_HA08N	P1.F11	13
D1	HPC_HA11P	P1.J12	13
	HPC_HA11N	P1.J13	13
A0	HPC_HA12P	P1.F13	13
	HPC_HA12N	P1.F14	13
B0	HPC_HA14P	P1.J15	13
	HPC_HA14N	P1.J16	13
C0	HPC_HA15P	P1.F16	13
	HPC_HA15N	P1.F17	13
D0	HPC_HA19P	P1.F19	14
	HPC_HA19N	P1.F20	14

**BOARD OUTLINE AND DIMENSIONS:**

*TOP VIEW*



All dimensions use the bottom left corner of the board as the origin. All dimensions are in millimeters (mm). Board thickness is 1.62 mm.

**Board Edge Lengths**

Edge	Length	Edge	Length	Edge	Length
<b>a</b>	69	<b>b</b>	61.7	<b>c</b>	2.4
<b>od</b>	9.1	<b>e</b>	2.1	<b>f</b>	8
<b>g</b>	61	<b>h</b>	21.9	<b>i</b>	3
<b>j</b>	56.9	Width	69	Height	78.8

⊗ **FMC Connector Mount Hole Locations ( x, y )**

73, 18.4	136, 18.4	3, 18.4	66, 18.4
----------	-----------	---------	----------

**SMA Locations ( x, y )**

<b>CKI</b>	118.6, 69.3
<b>OA_P</b>	61.7, 69.3
<b>OA_N</b>	92.1, 69.3

***Euvis Inc.***

Ordering Information:

Email to: [Sales@euvis.com](mailto:Sales@euvis.com)

Or call: (805) 583-9888 x108 Sales Department

Or fax: (805) 583-9889

The information contained in this document is based on preliminary measured results. Characteristic data and other specifications are subject to change without notice. Customers are advised to confirm information in this advanced datasheet prior to using this information or placing the order.

Euvis Inc. does not assume any liability arising from the application or use of any product or circuit described herein, neither does it convey any license under its patents or any other rights.