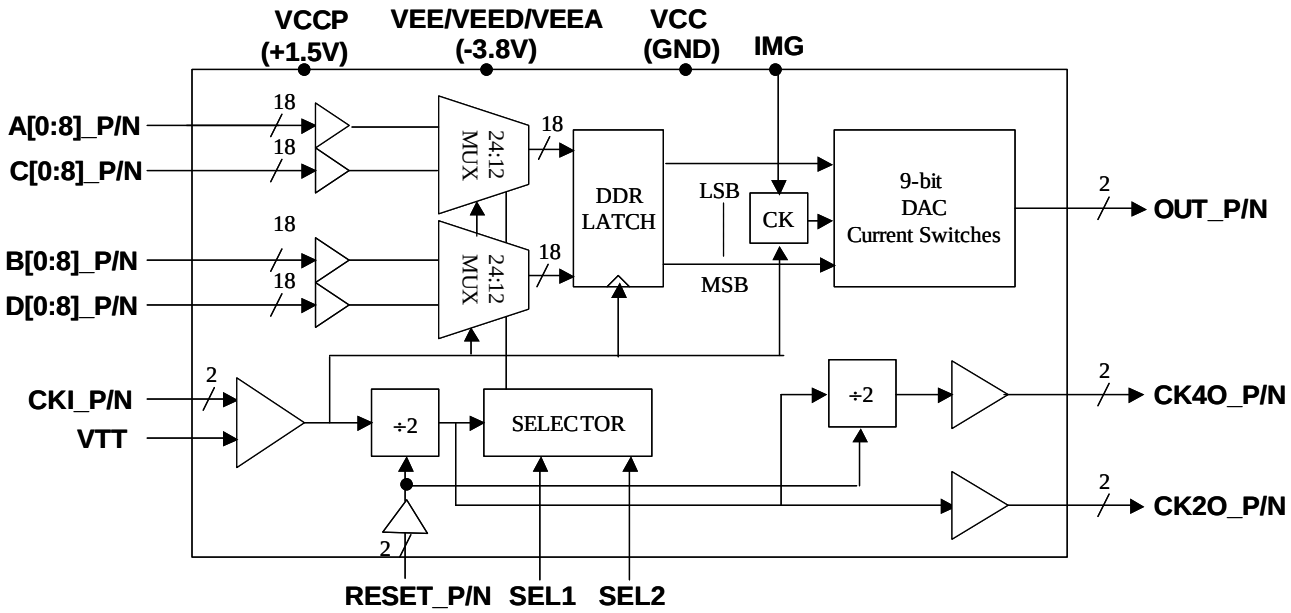
MD6639 : *Double Sampling Rate > 10.0 Gsps Broadband 5GH Bandwidth MUXDAC*



KEY FEATURES

- 4:1 multiplexing ratio for each input bit of DAC
- 9-bit Double Sampling Rate (DSR) DAC enables analog output sampling rate twice of the clock rate
- Clock rate up to 5 GHz with DAC analog output sampling rate up to 10 Gsps
- Ultra wideband with bandwidth from DC up to 5 GHz
- Complementary outputs with 50-Ω back terminations
- Both complementary divide-by-2 and divide-by-4 clock outputs are provided for data synchronization
- The duty cycle of the clock driving DAC can be adjusted by IMG pin to minimize the image signal due to double sampling
- Variable 400~800 mV_{pp} single-ended output swing
- On-chip 100 ohm termination between each differential input data and RESET pair
- Ultra Low Latency: 3 clock cycles or less counted from data sampling point
- Ultra Low Phase Noise
- 3.1 W power consumption
- EAR99: No export license required

Description

The **MD6639** is a high-speed 9-bit Digital to Analog Converter (DAC) integrated with 4:1 multiplexer for each DAC input bit. The digital data inputs are LVDS with on-chip 100 ohm termination resistors. The Double Sampling Rate (DSR) DAC enables its analog output sampling rate twice of the clock rate. The device can be clocked up to 5 GHz to

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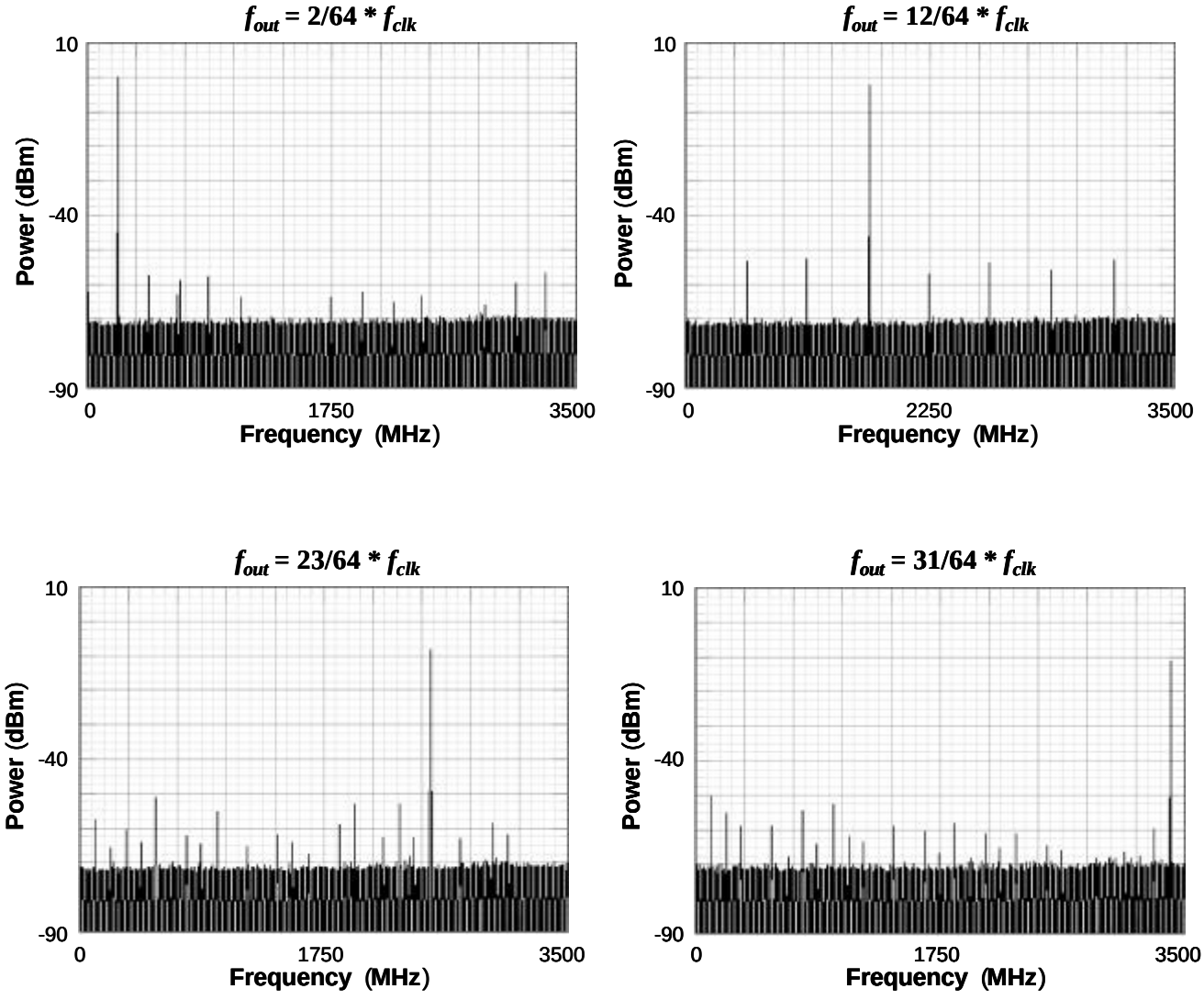
achieve 10 Gsps at DAC analog outputs. Complementary analog outputs are available with 50-Ω output back terminations. Divided-by-2 and Divide-by-4 clock LVDS outputs (**CK2O_P/N** & **CK4O_P/N**) and sampling phase selection (**SEL1/SEL2**) are provided to ease the alignment of sampling phase relative to the input data. An **IMG** pin is provided to adjust the duty cycle of the clock driving DAC to minimize the image signal due to double sampling.

Representative Measured RF Spectrum

7 Gsps with f_{clk} = 3.5 GHz



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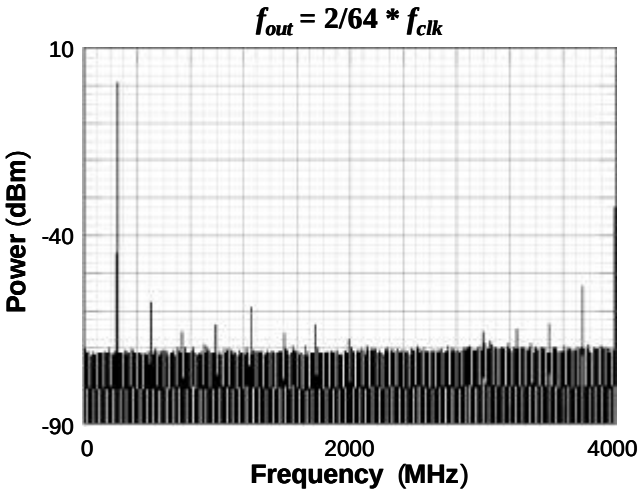
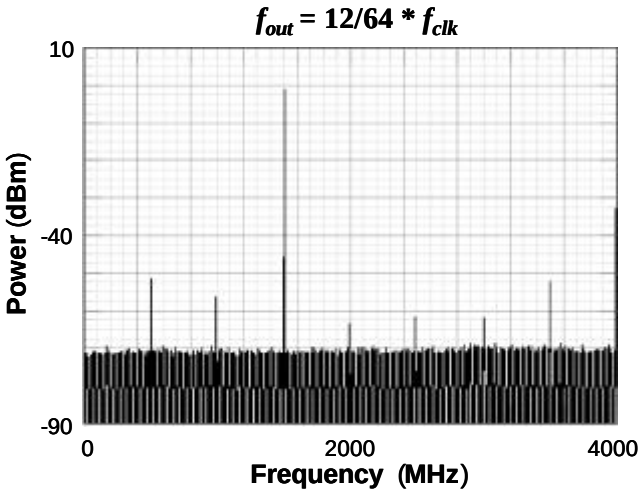
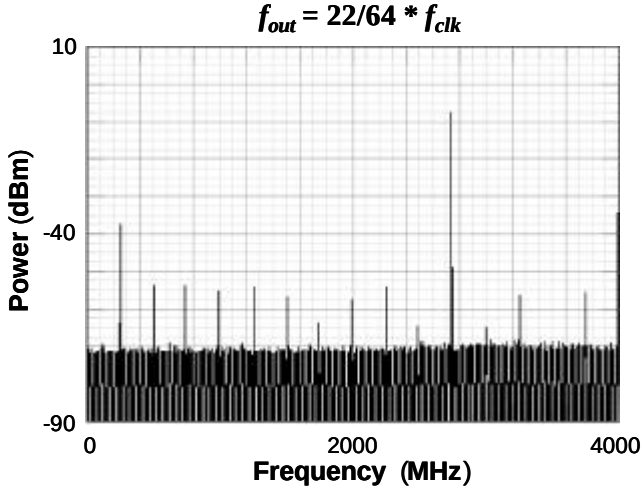
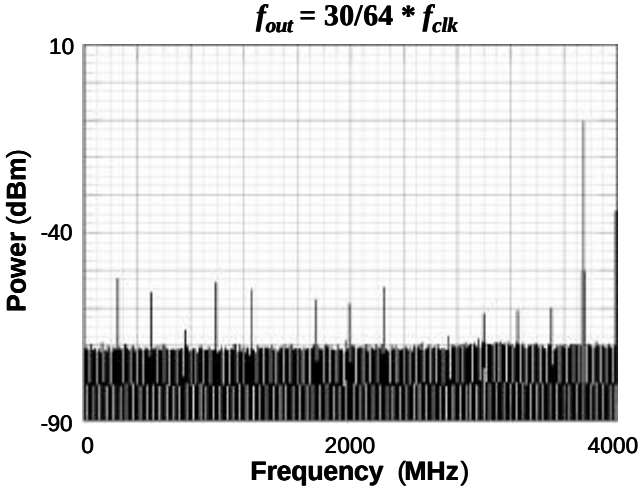
8 Gsps with f_{clk} = 4.0 GHz



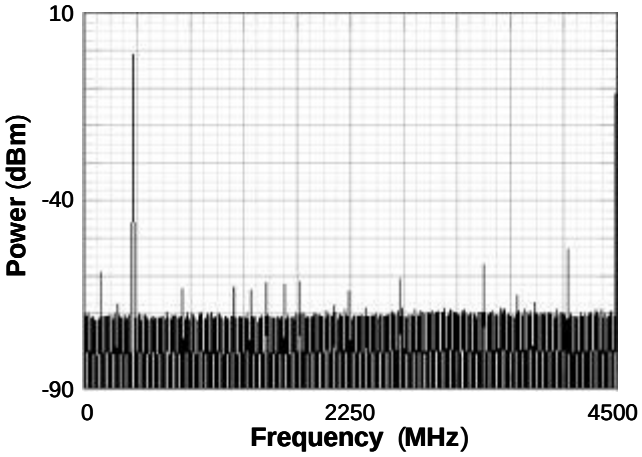




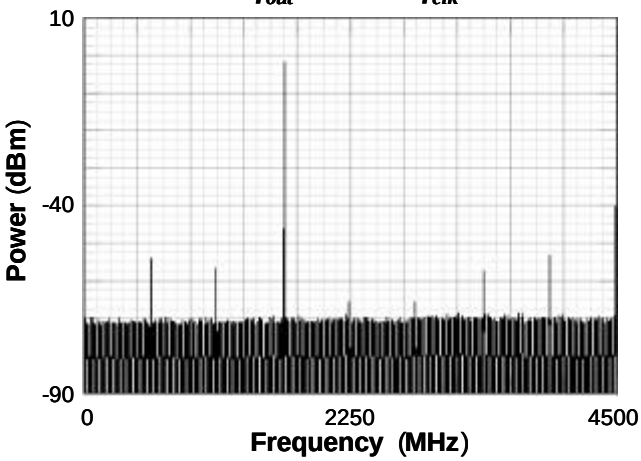


9 Gsps with f_{clk} = 4.5 GHz

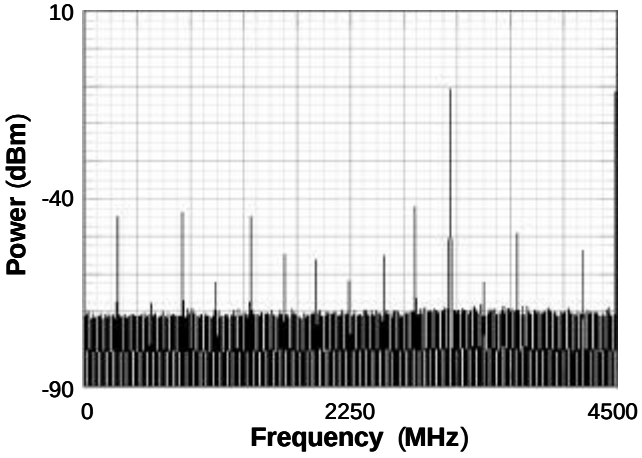
f_{out} = 3/64 * f_{clk}



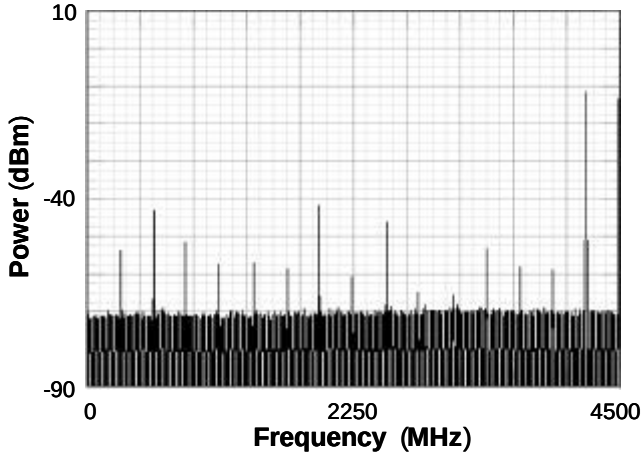
f_{out} = 12/64 * f_{clk}



f_{out} = 22/64 * f_{clk}



f_{out} = 30/64 * f_{clk}



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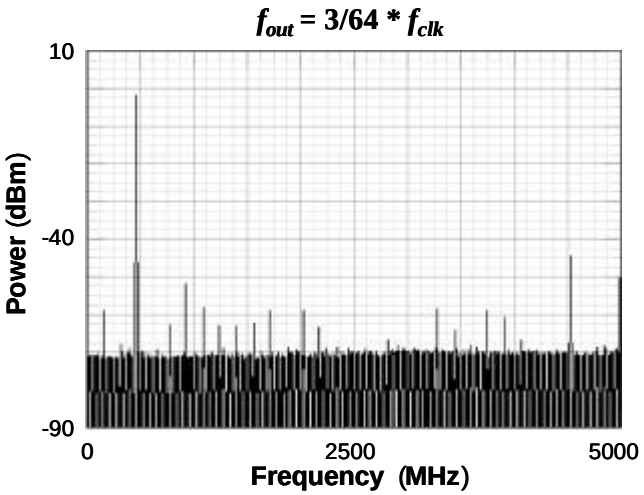
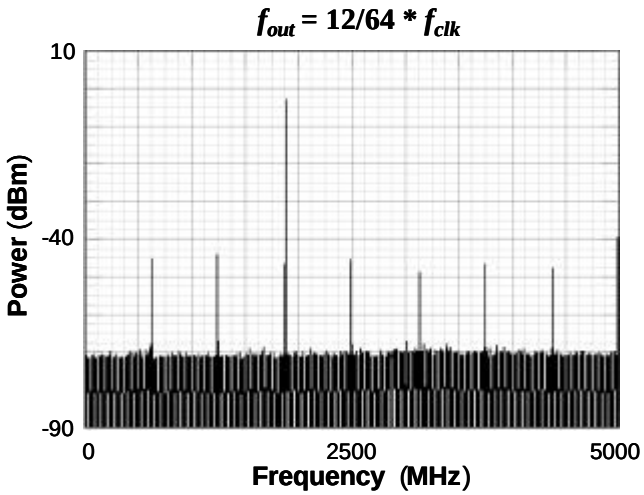
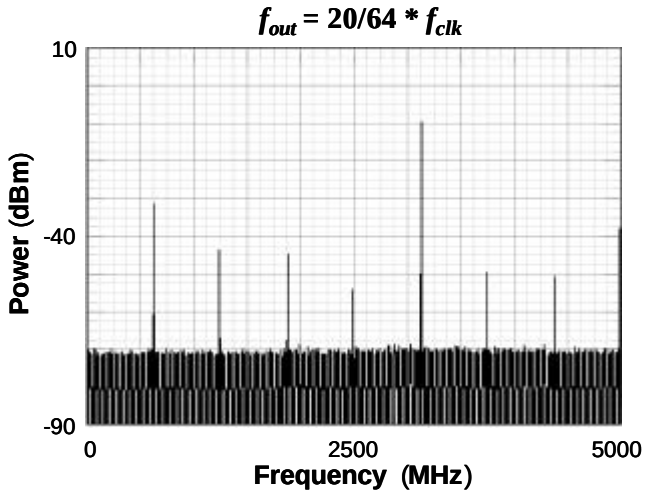
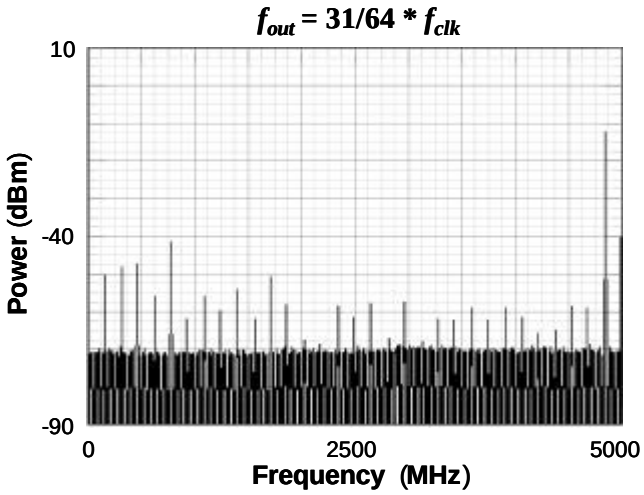
10 Gsps with f_{clk} = 5.0 GHz









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