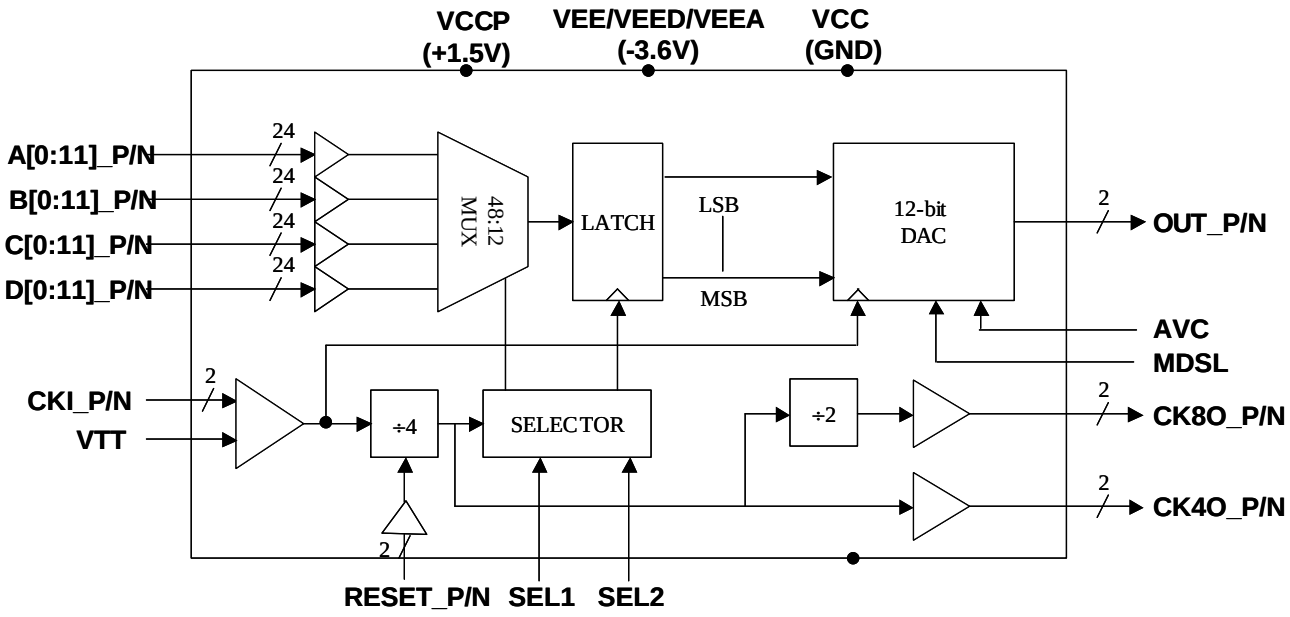
MD657B : *High-Speed > 6.0 GHz Broadband MUXDAC with Analog Output Mode Selections*



KEY FEATURES

- 4:1 multiplexing ratio for each input bit of DAC
- 12-bit resolution DAC up to > 6**.0 Gsps rate**
- DAC analog output format can be selected between Normal-Hold **(NH) mode** or Return-to-Zero **(RZ) mode**
- Complementary outputs with 50-Ω back terminations
- Both complementary divide-by-4 and divide-by-8 clock outputs are provided for data synchronization
- 2.75 W power consumption
- Variable 400~800 mV_{pp} single-ended output swing
- On-chip 100 ohm termination between each differential input data and RESET pair
- Ultra Low Latency: 5 clock cycles or less counted from data sampling point
- Ultra Low Phase Noise
- LQFP package with exposed pad

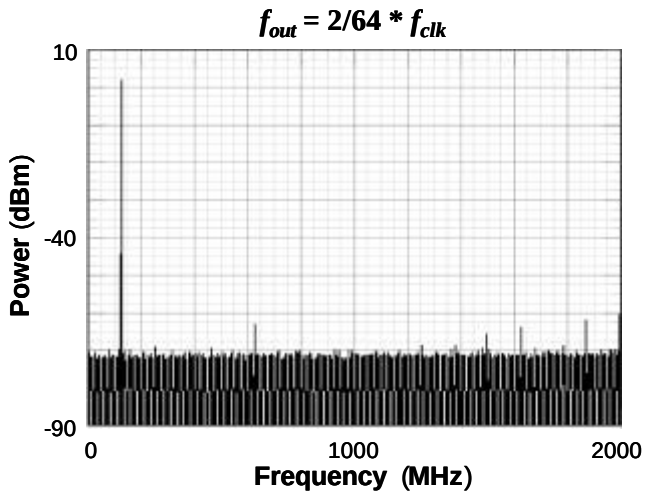
Description

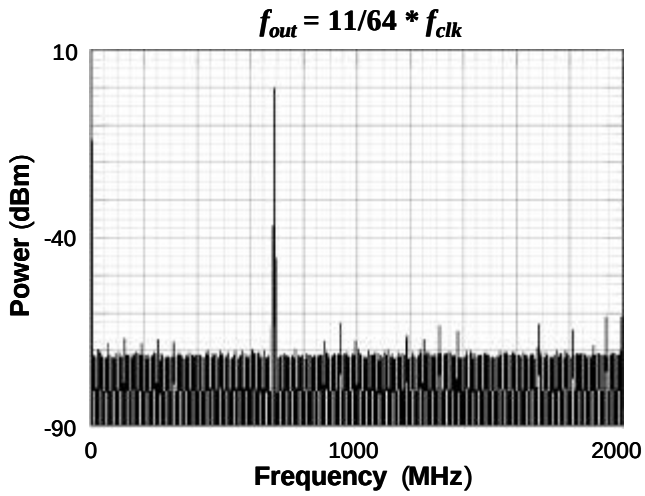
MD657B is a high-speed 12-bit Digital to Analog Converter (DAC) integrated with a 48:12 (12 channels of 4:1) input multiplexer. The on-chip DAC can be operated at a sampling rate > 6.0 Gsps. The analog outputs of DAC can be selected between Normal-Hold mode (for the 1st Nyquist band) or Return-to-Zero mode (for the 1st, 2nd and 3rd Nyquist band) operation. The differential digital data input interfaces are LVPECL, LVDS, and CML compatible. After the 48 pairs of differential data inputs were multiplexed up to 4 times of speed, the 12 high speed data bits are latched and encoded to drive DAC output stage. Complementary outputs are available with 50-Ω output back terminations. Divided-by-4 clock outputs and sampling phase selection (SEL1 and SEL2) are provided to ease the alignment of sampling phase relative to the input data. Divided-by-8 clock

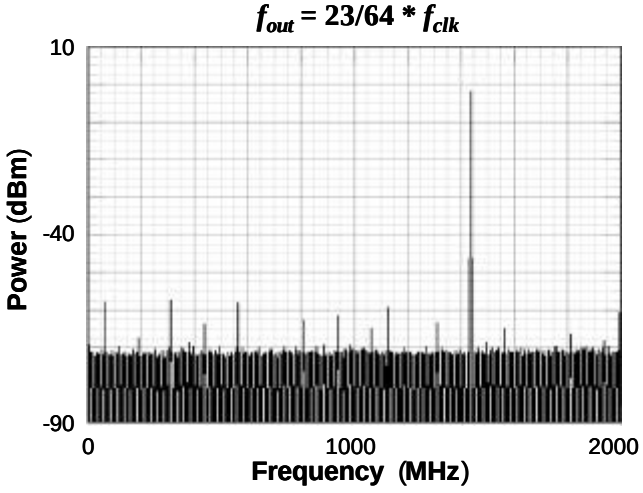
outputs are also provided. A RESET function is provided for system applications which need to synchronize the outputs from multiple **MD657B**'s.

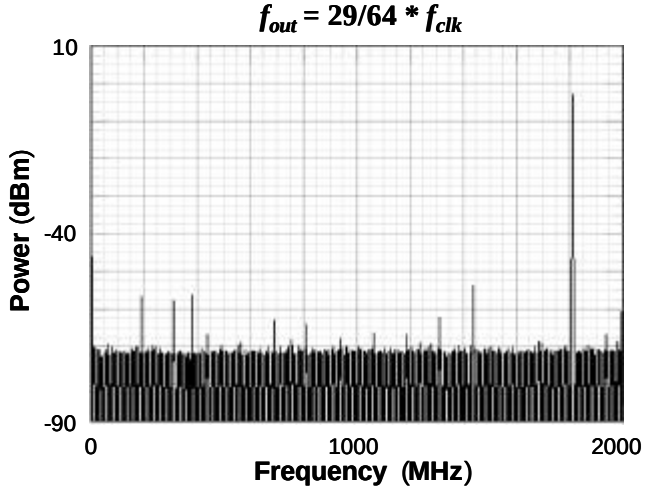
Representative Measured RF Spectrum

f_{clk} = 4.0 GHz









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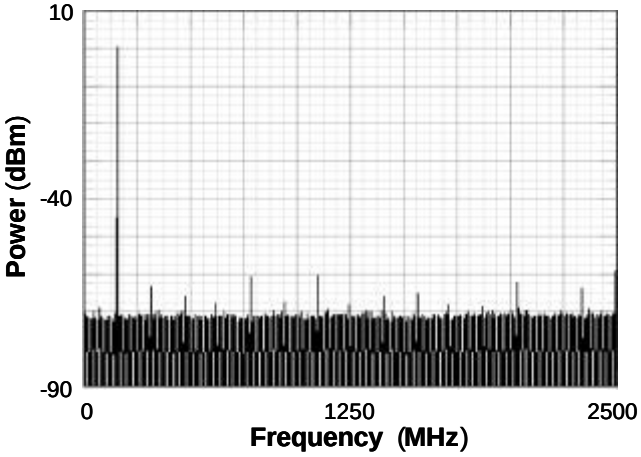
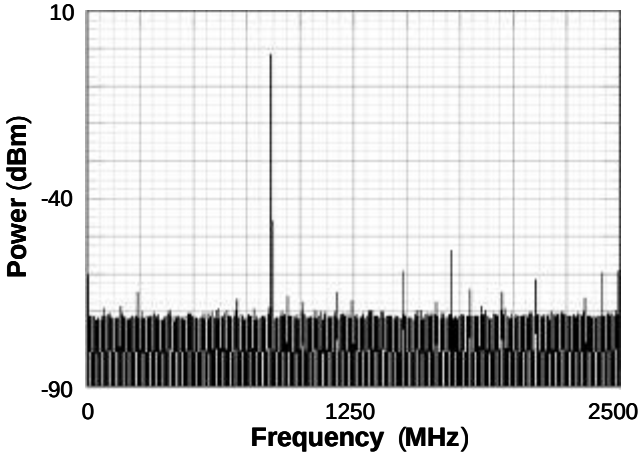
f_{clk} = 5.0 GHz

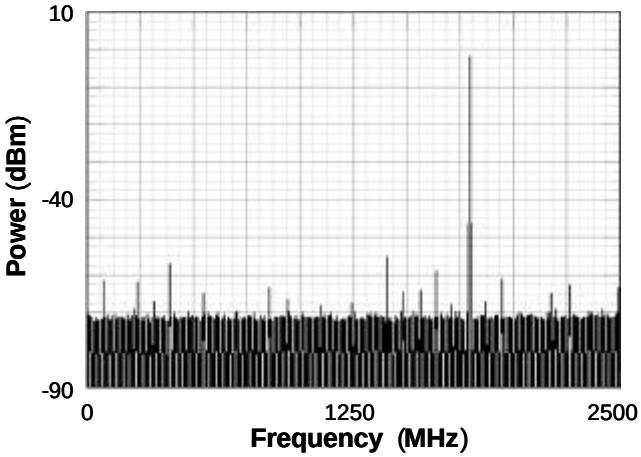
f_{out} = 2/64 * f_{clk}



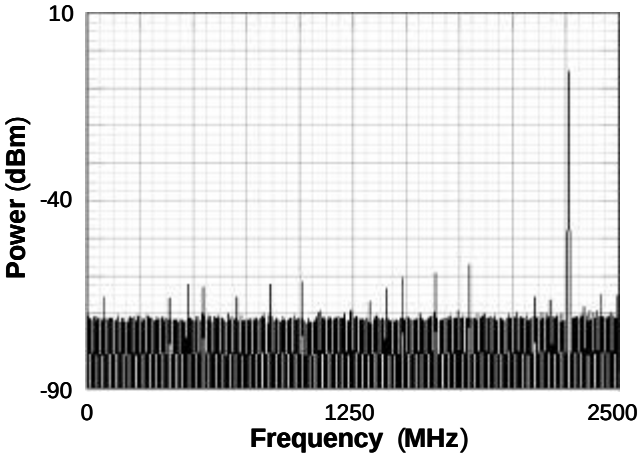
f_{out} = 11/64 * f_{clk}



f_{out} = 23/64 * f_{clk}



f_{out} = 29/64 * f_{clk}



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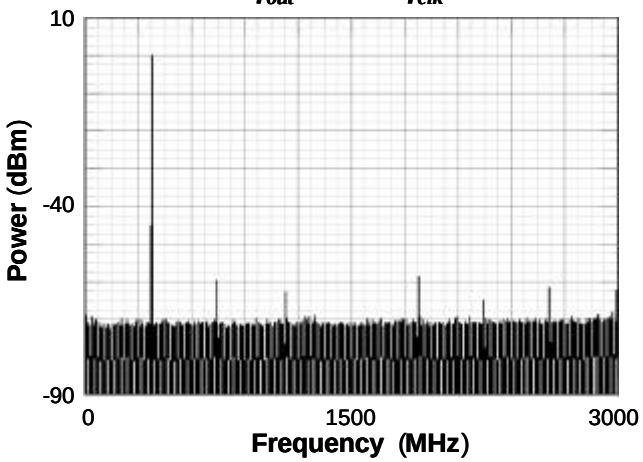
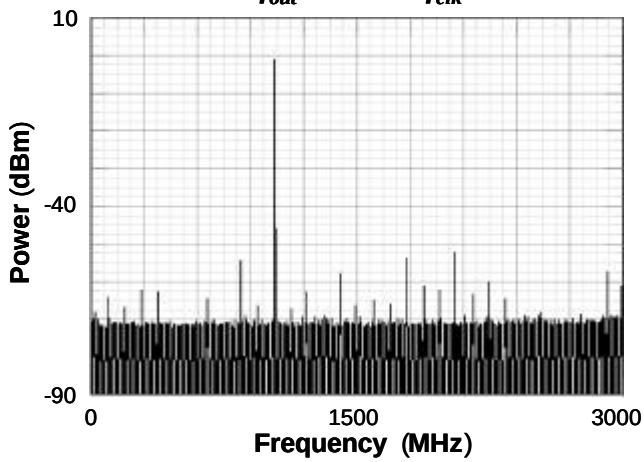
f_{clk} = 6.0 GHz

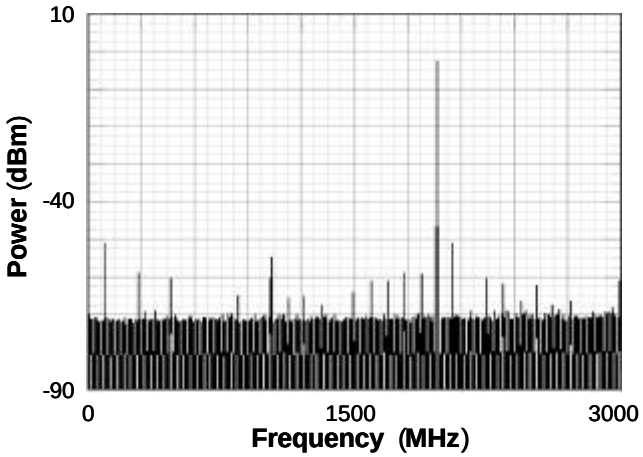
f_{out} = 4/64 * f_{clk}



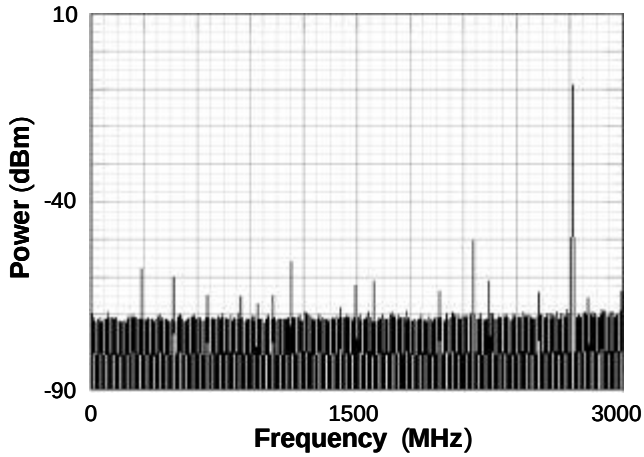
f_{out} = 11/64 * f_{clk}



f_{out} = 21/64 * f_{clk}



f_{out} = 29/64 * f_{clk}



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