

8GHz Programmable Divide-by-128 to 255 DV255N

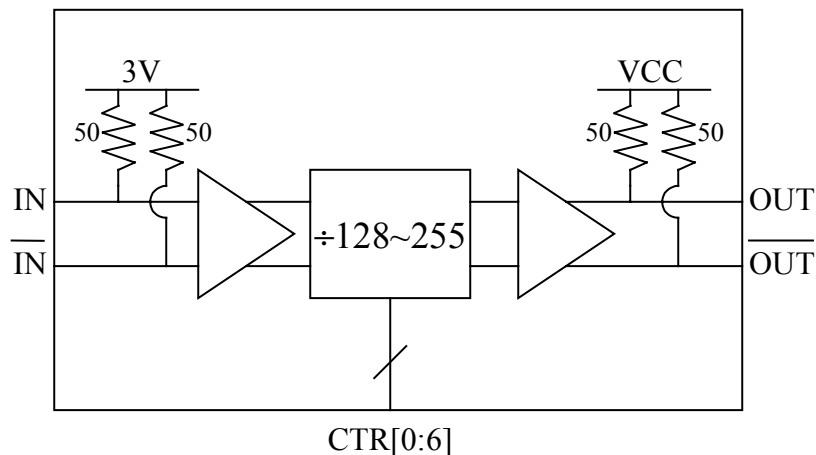
PRODUCT DESCRIPTION

DV255N is a high-speed programmable modulus (128 to 255) static divider in 24-pin 4x4mm plastic QFN package. Due to its high input sensitivity, low output phase noise, and small size, DV255N is well suited for wide-range of applications from communications, instrumentation, radios/radar, to medical etc. It has differential input and output and accepts input frequency from 0.2GHz (sine wave, DC for square wave) to 8GHz. Seven TTL/LVTTL-compatible modulus control pins are provided to select desired modulus between 128 and 255. A single power supply of +5V is required.

KEY FEATURES

- 0.2-8GHz Bandwidth
- Programmable modulus of 128 to 255
- Low phase noise: -140 dBc/Hz
- High input sensitivity: -25 dBm
- Output amplitude: 800 mVp-p (differential)
- Differential input and output
- 50Ω input/output impedance
- Single power supply: +5V
- Current consumption: 150mA
- 24-pin 4x4mm plastic QFN package

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Room temperature, $Z_0=50\Omega$, $V_{cc}=+5V$

Parameter	Conditions	Min	Typical	Max	Units
Ambient Temperature		-40	25	85	°C
Max input frequency	Sine wave input		8		GHz
Min input frequency ¹	Sine wave input		0.2		GHz
Input power ²	$f_{in}=0.2-8GHz$, single ended	-25		10	dBm
Output amplitude 1	$f_{in}=8GHz$, single ended		400		mVp-p
Output amplitude 2	$f_{in}=8GHz$, differential		800		mVp-p
Feedthrough	Input frequency at output		-25		dB
Reverse isolation	< 8GHz		30		dB
Phase noise	SSB 100kHz offset		-140		dBc/Hz
Output rise/fall time	20% to 80%		50		ps
Input/output return loss	< 8GHz		12		dB
Output Impedance	DC, output pin to V_{cc}	45	50	55	Ω
Control Low Level ³	DC, control pin to GND	-0.3	0	0.3	V
Control High Level ³	DC, control pin to GND	1.0	2.0	3.5	V
Current Consumption			150		mA

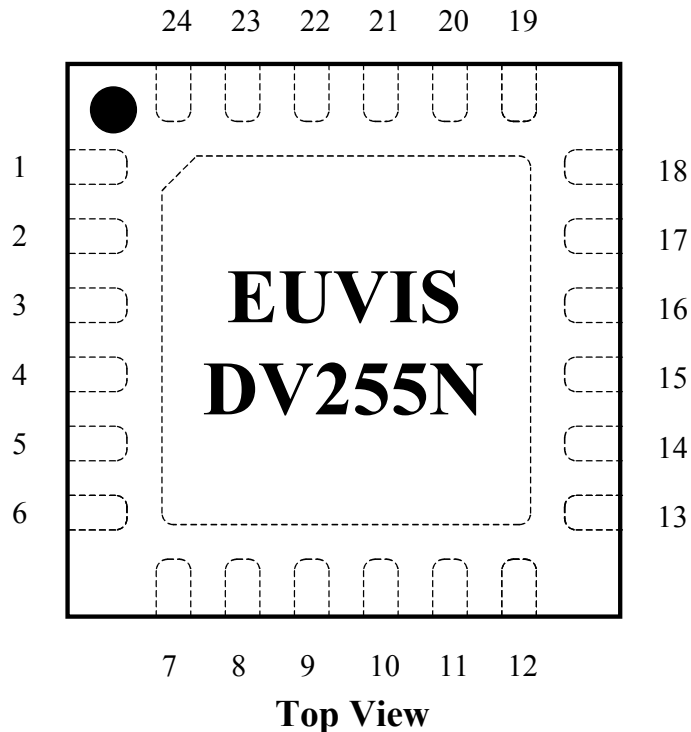
¹ Minimum input frequency is DC with square-wave input signal.² AC coupling is recommended for input signals. Common mode voltage of 3V is required for DC-coupled input signals in order to match internal input bias of 3V.³ CTR[0:6] modulus control pins.

PIN DESCRIPTION

Pin No.	Name	Signal
1, 3, 5, 6, 13, 14, 18	GND	Ground
2	IN	Input
4	IN_	Complimentary input
7, 11, 12, 16, 20, 24	VCC	Positive power supply (+5V)
8	CTR0	TTL/LVTTL-compatible modulus control 0
9	CTR1	TTL/LVTTL-compatible modulus control 1
10	CTR2	TTL/LVTTL-compatible modulus control 2
15	OUT	Divided output
17	OUT_	Divided complimentary output
19	CTR6	TTL/LVTTL-compatible modulus control 6
21	CTR5	TTL/LVTTL-compatible modulus control 5
22	CTR4	TTL/LVTTL-compatible modulus control 4
23	CTR3	TTL/LVTTL-compatible modulus control 3

PIN ASSIGNMENT

- Package type: 24-pin 4mm x 4mm plastic QFN
- Thickness: 1mm



MODULUS FORMULA

Modulus = $128 + \langle C0 \rangle \bullet 1 + \langle C1 \rangle \bullet 2 + \langle C2 \rangle \bullet 4 + \langle C3 \rangle \bullet 8 + \langle C4 \rangle \bullet 16 + \langle C5 \rangle \bullet 32 + \langle C6 \rangle \bullet 64$

$\langle C^* \rangle$ is **1** when CTR* potential is TTL/LVTTL high; **0** when CTR* potential is TTL/LVTTL low

When all modulus controls are logic low, a modulus of 128 is selected. When all modulus controls are logic high, a modulus of 255 is selected.

ORDERING INFORMATION

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