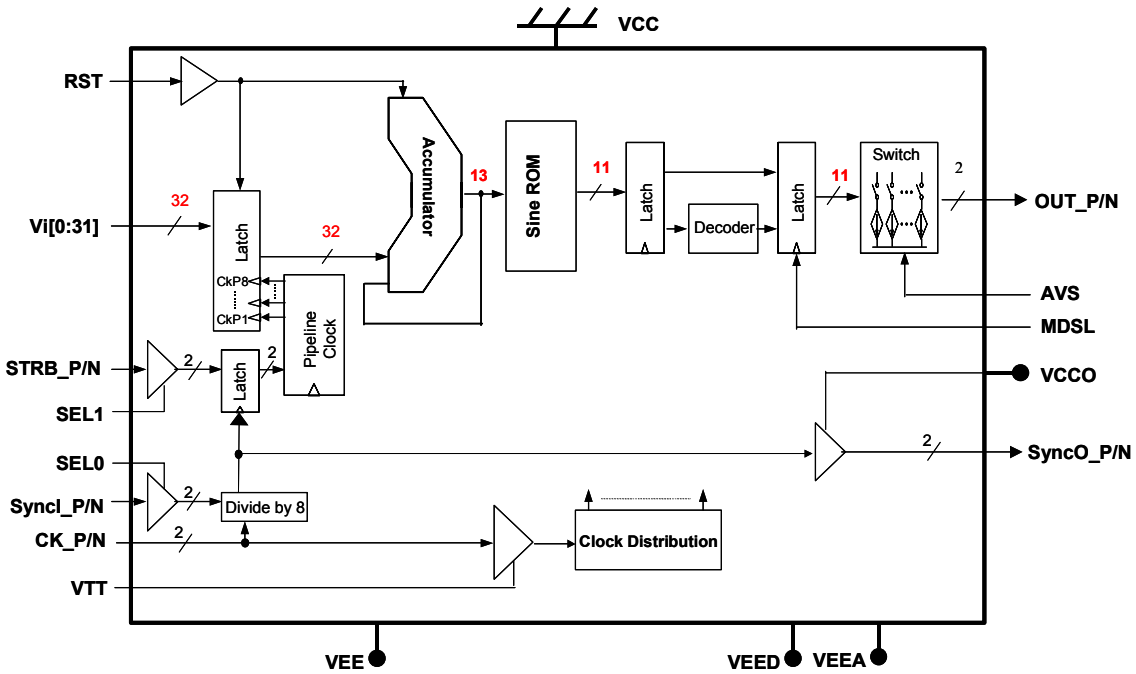
DS872 – *Direct Digital Synthesizer for High Speed Chirping*



KEY FEATURES

- 32-bit frequency tuning word
- 13-bit ROM phase address resolution
- On chip 11-bit DAC
- Clock rate up to 3.2 GHz
- Analog outputs selectable between Normal-Hold format and Return-to-Zero format
- Sine wave generation up to 1.5 GHz 1st Nyquist band for Normal-Hold mode or 4.5 GHz 3rd Nyquist band for Return-to-Zero mode.
- Broadband worst SFDR > 50 dBc (DC to 1.5-GHz Bandwidth) at a 3 GHz clock rate
- Complementary analog waveform outputs with 50 Ω back terminations
- **SyncI_P/N** synchronizes multiple chip applications
- **SyncO_P/N** provides reference for data loading and synchronizes STROBE signals.
- LVTTL/CMOS digital pattern control input
- Asynchronous Reset (**RST**) pin to initiate phase 0 starting state
- Strobe inputs (**STRB_P/N**) to update the frequency word and DAC output frequency
- Wide data loading window allow **DS872** to be controlled by memory, micro-controller, FPGA or DSP chips to update frequency word as fast as 8 clock cycles without clock slipping or glitches during frequency transition
- 3.6 W power consumption with a single -5V power supply
- 64-pin QFN package

685 Cochran Street, Suite 160, Simi Valley, CA 93065
Email: sales@euvis.com Web: www.euvis.com Tel.: (805) 583-9888

Description

The **DS872** is a high-speed Direct Digital Synthesizer (DDS) with a frequency tuning resolution of 32 bits, ROM phase resolution of 13-bit and a DAC amplitude resolution of 11 bits. The analog outputs of DAC can be selected between Normal-Hold mode (for the 1st Nyquist band) and Return-to-Zero mode (for the 1st, 2nd and 3rd Nyquist band) operation. Sine waves can be generated up to 1st Nyquist band near 1.5 GHz (at a 3-GHz clock rate) with Normal-Hold mode of DAC or up to 3rd Nyquist band around 4.5 GHz with Return-to-Zero mode of DAC. The initial phase can be reset to zero degrees to start with. The chip has a pair of complementary analog outputs with 50-Ω back terminations. The frequency of output waveforms can be controlled by thirty-two frequency control bits, **Vi[0:31]**. The **DS872** accepts either differential clock inputs or a single-ended clock input and features 50-Ω on-chip back terminations with user-defined threshold. The frequency resolution bits accept LVTTL or CMOS input levels. Differential synchronization input **SyncI_P/N** provides synchronization for multiple chip applications and start each chip ready to accept frequency word inputs. The synchronous Strobe inputs are latched by the transition edges of internal generated divide-by-8 clocks which were also sent to the output pins **SyncO_P/N**. **SyncO_P/N**. can be used as a reference to synchronize the frequency word and strobe signal input timing alignment to the internal divide-by-8 clocks to latch properly. The Reset is asynchronous to minimize clock latencies of effectiveness on the analog outputs. The internal timing was optimized to avoid clock slipping during frequency word transition or after reset. Only a single –5V power supply is required.

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